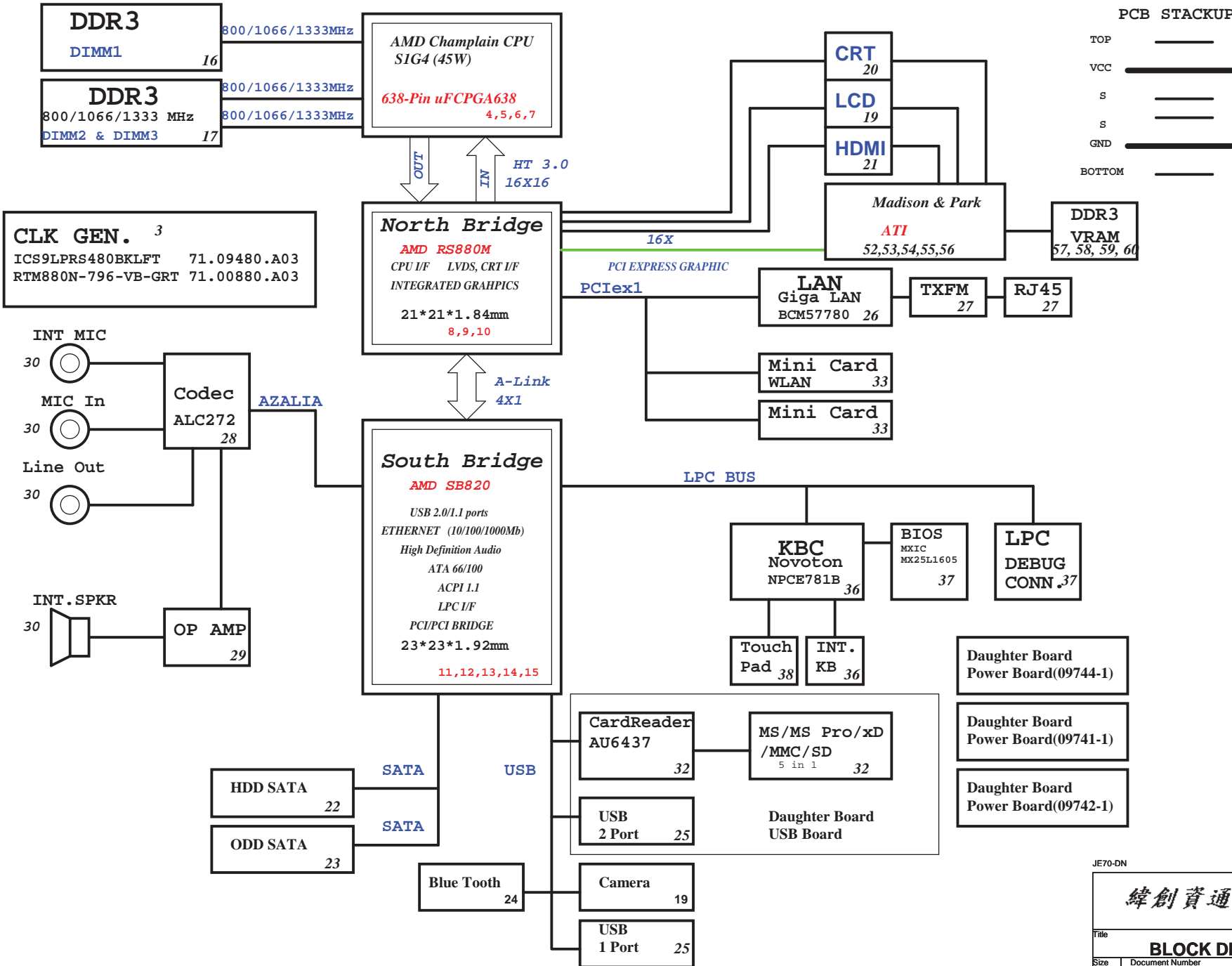


JE70-DN/SJV71-DN/HM72-DN Block Diagram

Project code: 91.4HP01.001
PCB P/N : 48.4HP01.011
REVISION : 09929-1



SYSTEM DC/DC RT8223 45	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)

SYSTEM DC/DC RT8209E 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8015A 47	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0

RT9025 48	
5V_S5	1D05V_S0

RT9161 48	
3D3V_S0	2D5V_S0 (200mA)

RT9025 48	
3D3V_S0	1V_VGA (1.2A)

RT9025,RT8209E 47	
3D3V_S5	1D1V_S5
5V_S5	1D1V_S0

CHARGER BQ24745 49	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A
	VCC_CORE_S0_1 0~1.55V 18A
	VDDNB 0~1.55V 18A

EC Functional Strap Definitions

page9

STRAP_DEBUG_BUS_GPIO_ENABLEb Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#) *1 :Disable 0 : Enable
RS780: Enables Side port memory (RS880 use HSYNC#) *1 :Disable 0 : Enable
SUS_STAT# Selects Loading of STRAPS From EEPROM *1 : Bypass the loading of EEPROM straps and use Hardware Default Values 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

page15

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

page15

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200	GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM	
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	

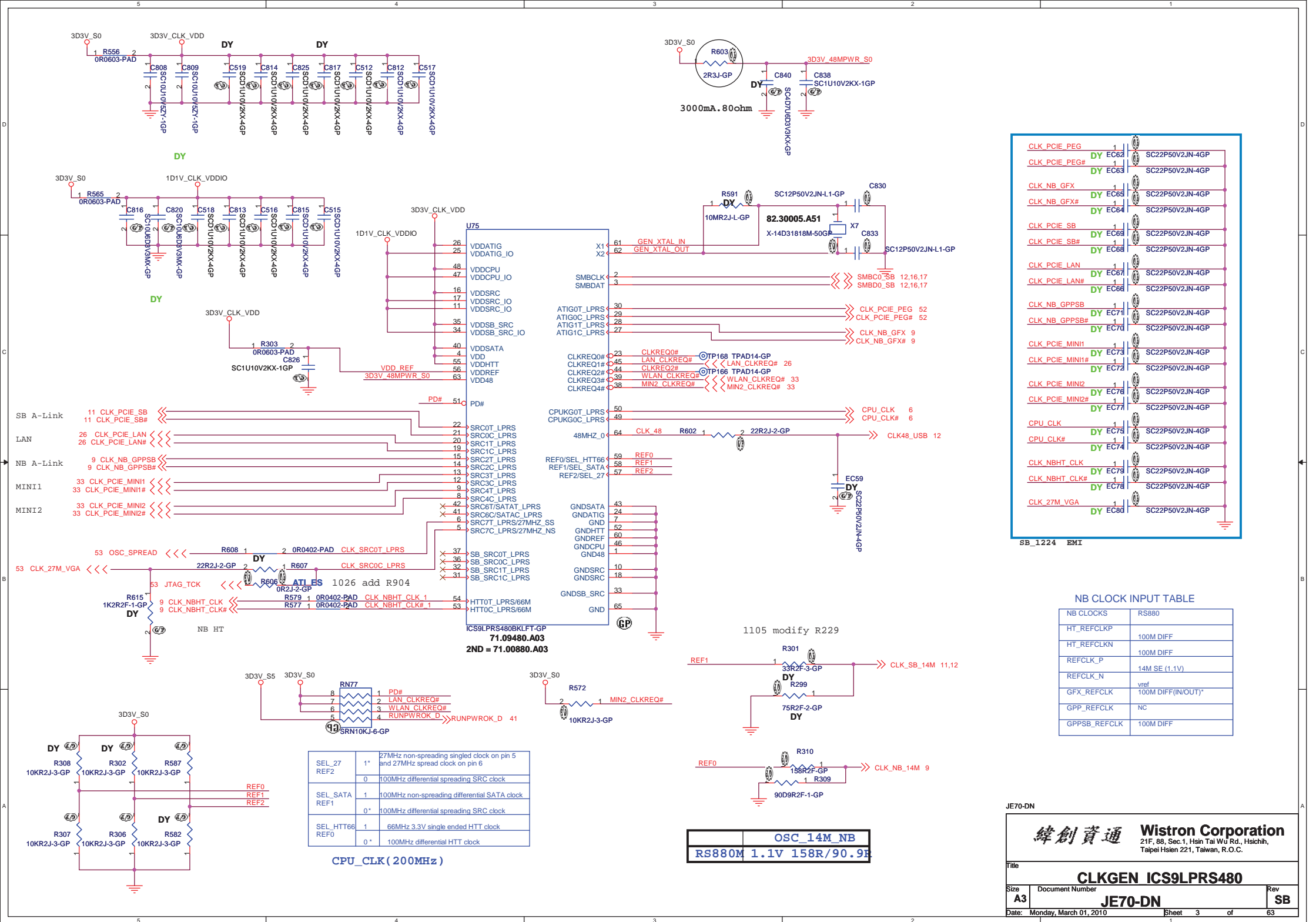
NOTE: SB820 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

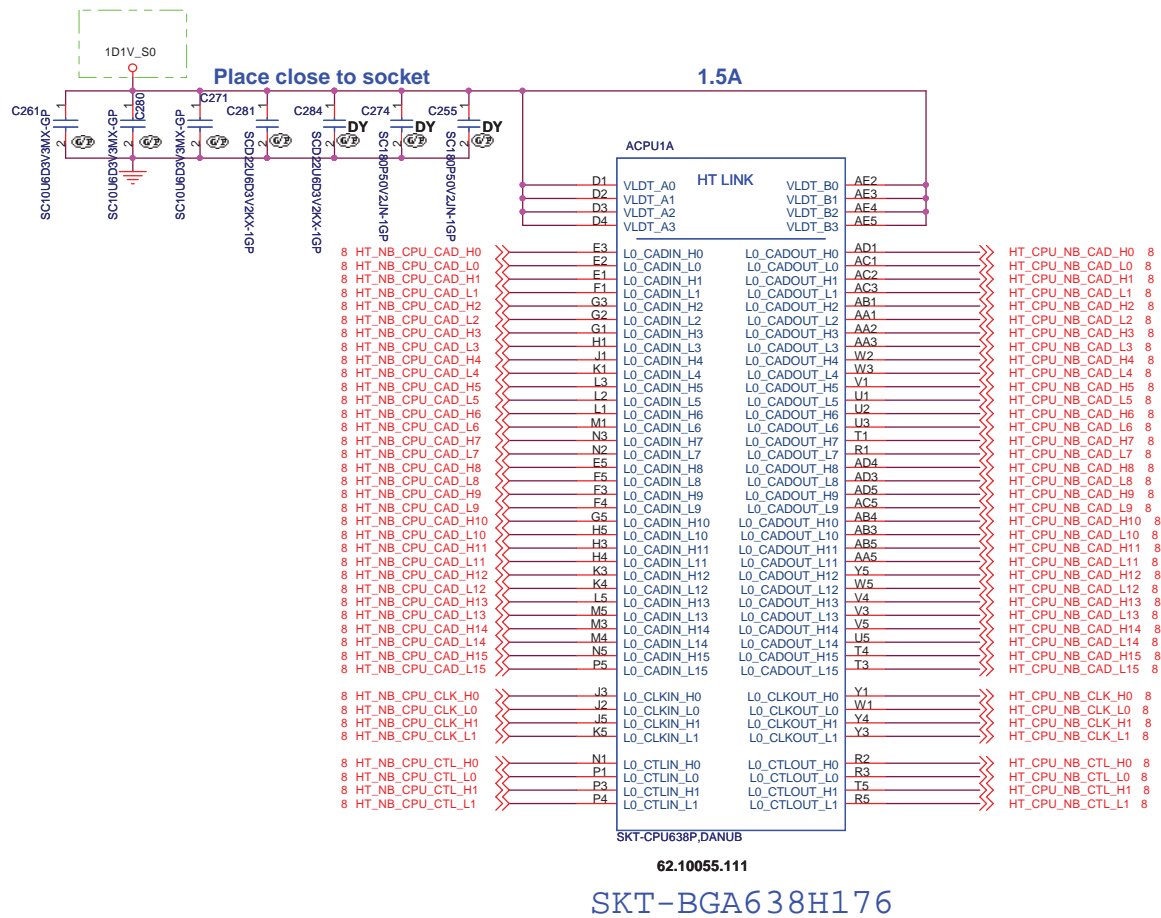
page12

	USB	
	Pair	Device
OCP3#	12	MINI2 CARD
	11	NC
	10	NC
	9	CCD
	8	NC
	7	Bluetooth
	6	USB3
	5	USB2
	4	CardReader
OCP2#	3	NC
	2	USB4
OCP0#	1	MINI1 CARD
	0	USB1

JE70-DN

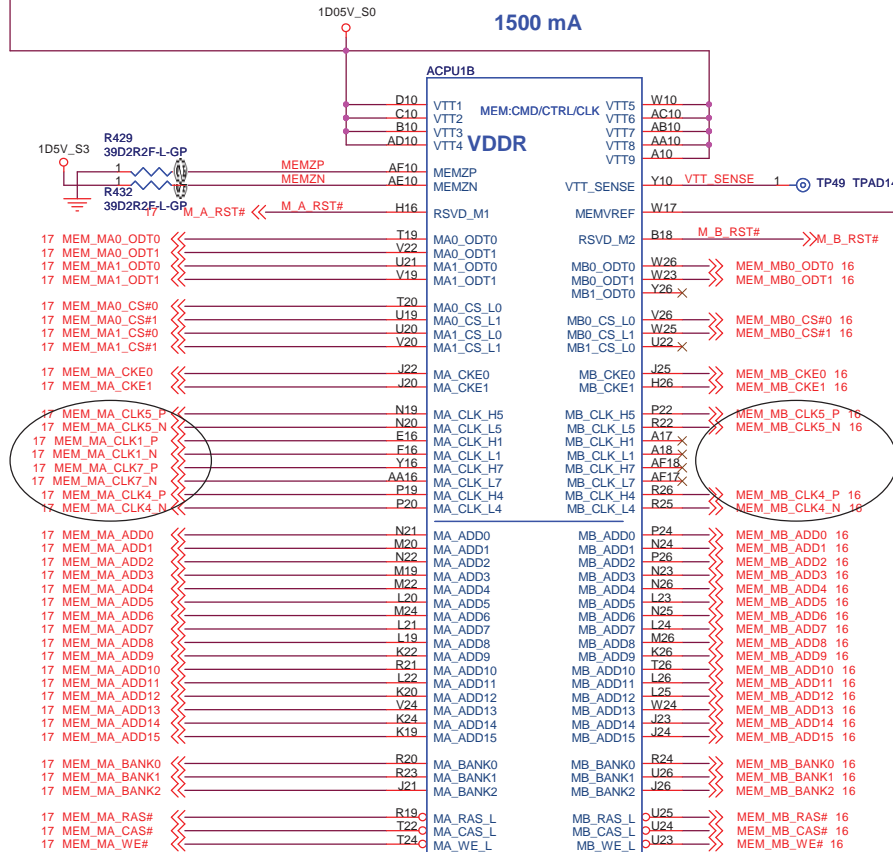
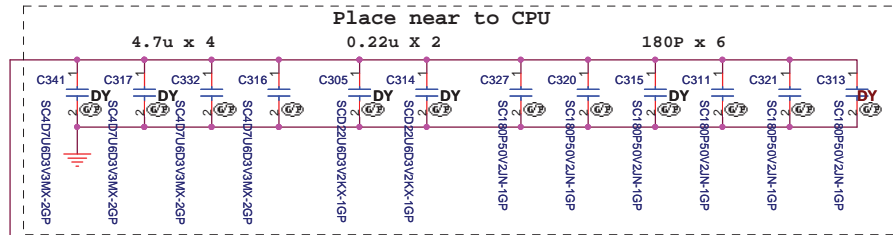
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Reference	
Size A3	Document Number JE70-DN
Date: Thursday, November 19, 2009	Rev SB
Sheet 2 of 63	



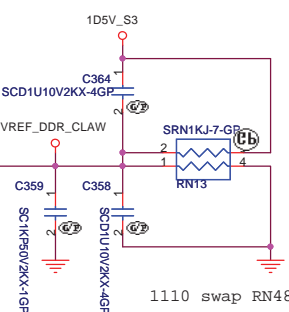


JE70-DN

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU HT LINK I/F (1/4)			
Size A3	Document Number JE70-DN		Rev SB
Date: Monday, March 01, 2010		Sheet 4 of 63	63



CLOSE TO CPU



1110 swap RN48

17	MEM_MA_DATA0	
17	MEM_MA_DATA1	
17	MEM_MA_DATA2	
17	MEM_MA_DATA3	
17	MEM_MA_DATA4	
17	MEM_MA_DATA5	
17	MEM_MA_DATA6	
17	MEM_MA_DATA7	
17	MEM_MA_DATA8	
17	MEM_MA_DATA9	
17	MEM_MA_DATA10	
17	MEM_MA_DATA11	
17	MEM_MA_DATA12	
17	MEM_MA_DATA13	
17	MEM_MA_DATA14	
17	MEM_MA_DATA15	
17	MEM_MA_DATA16	
17	MEM_MA_DATA17	
17	MEM_MA_DATA18	
17	MEM_MA_DATA19	
17	MEM_MA_DATA20	
17	MEM_MA_DATA21	
17	MEM_MA_DATA22	
17	MEM_MA_DATA23	
17	MEM_MA_DATA24	
17	MEM_MA_DATA25	
17	MEM_MA_DATA26	
17	MEM_MA_DATA27	
17	MEM_MA_DATA28	
17	MEM_MA_DATA29	
17	MEM_MA_DATA30	
17	MEM_MA_DATA31	
17	MEM_MA_DATA32	
17	MEM_MA_DATA33	
17	MEM_MA_DATA34	
17	MEM_MA_DATA35	
17	MEM_MA_DATA36	
17	MEM_MA_DATA37	
17	MEM_MA_DATA38	
17	MEM_MA_DATA39	
17	MEM_MA_DATA40	
17	MEM_MA_DATA41	
17	MEM_MA_DATA42	
17	MEM_MA_DATA43	
17	MEM_MA_DATA44	
17	MEM_MA_DATA45	
17	MEM_MA_DATA46	
17	MEM_MA_DATA47	
17	MEM_MA_DATA48	
17	MEM_MA_DATA49	
17	MEM_MA_DATA50	
17	MEM_MA_DATA51	
17	MEM_MA_DATA52	
17	MEM_MA_DATA53	
17	MEM_MA_DATA54	
17	MEM_MA_DATA55	
17	MEM_MA_DATA56	
17	MEM_MA_DATA57	
17	MEM_MA_DATA58	
17	MEM_MA_DATA59	
17	MEM_MA_DATA60	
17	MEM_MA_DATA61	
17	MEM_MA_DATA62	
17	MEM_MA_DATA63	
17	MEM_MA_DM0	
17	MEM_MA_DM1	
17	MEM_MA_DM2	
17	MEM_MA_DM3	
17	MEM_MA_DM4	
17	MEM_MA_DM5	
17	MEM_MA_DM6	
17	MEM_MA_DM7	
17	MEM_MA_DQS0_P	
17	MEM_MA_DQS0_N	
17	MEM_MA_DQS1_P	
17	MEM_MA_DQS1_N	
17	MEM_MA_DQS2_P	
17	MEM_MA_DQS2_N	
17	MEM_MA_DQS3_P	
17	MEM_MA_DQS3_N	
17	MEM_MA_DQS4_P	
17	MEM_MA_DQS4_N	
17	MEM_MA_DQS5_P	
17	MEM_MA_DQS5_N	
17	MEM_MA_DQS6_P	
17	MEM_MA_DQS6_N	
17	MEM_MA_DQS7_P	
17	MEM_MA_DQS7_N	

ACPU1C

MEM-DATA

G12	MA_DATA0	MB_DATA0	C11
F12	MA_DATA1	MB_DATA1	A11
H14	MA_DATA2	MB_DATA2	A14
G14	MA_DATA3	MB_DATA3	B14
H11	MA_DATA4	MB_DATA4	G11
C13	MA_DATA5	MB_DATA5	D12
E13	MA_DATA6	MB_DATA6	A13
H15	MA_DATA7	MB_DATA7	A15
E15	MA_DATA8	MB_DATA8	A16
E17	MA_DATA9	MB_DATA9	A19
H17	MA_DATA10	MB_DATA10	A20
H12	MA_DATA11	MB_DATA11	C14
F14	MA_DATA12	MB_DATA12	D14
C17	MA_DATA13	MB_DATA13	C18
G17	MA_DATA14	MB_DATA14	D18
G18	MA_DATA15	MB_DATA15	D20
C19	MA_DATA16	MB_DATA16	A21
D22	MA_DATA17	MB_DATA17	D24
E18	MA_DATA18	MB_DATA18	C25
F18	MA_DATA19	MB_DATA19	B20
MA_DATA20	MB_DATA20	C20	
MA_DATA21	MB_DATA21	B24	
MA_DATA22	MB_DATA22	C24	
MA_DATA23	MB_DATA23	E23	
MA_DATA24	MB_DATA24	C24	
MA_DATA25	MB_DATA25	G25	
MA_DATA26	MB_DATA26	G26	
MA_DATA27	MB_DATA27	C26	
MA_DATA28	MB_DATA28	D26	
MA_DATA29	MB_DATA29	G23	
MA_DATA30	MB_DATA30	C24	
MA_DATA31	MB_DATA31	AA24	
MA_DATA32	MB_DATA32	AA23	
MA_DATA33	MB_DATA33	AD24	
MA_DATA34	MB_DATA34	AE24	
MA_DATA35	MB_DATA35	AA26	
MA_DATA36	MB_DATA36	AA25	
MA_DATA37	MB_DATA37	AD26	
MA_DATA38	MB_DATA38	AE25	
MA_DATA39	MB_DATA39	AC22	
MA_DATA40	MB_DATA40	AD22	
MA_DATA41	MB_DATA41	AE20	
MA_DATA42	MB_DATA42	AF20	
MA_DATA43	MB_DATA43	AE24	
MA_DATA44	MB_DATA44	AE23	
MA_DATA45	MB_DATA45	AC20	
MA_DATA46	MB_DATA46	AD20	
MA_DATA47	MB_DATA47	AD18	
MA_DATA48	MB_DATA48	AE18	
MA_DATA49	MB_DATA49	AC14	
MA_DATA50	MB_DATA50	AD14	
MA_DATA51	MB_DATA51	AE19	
MA_DATA52	MB_DATA52	AC18	
MA_DATA53	MB_DATA53	AE16	
MA_DATA54	MB_DATA54	AE15	
MA_DATA55	MB_DATA55	AE13	
MA_DATA56	MB_DATA56	AC12	
MA_DATA57	MB_DATA57	AE11	
MA_DATA58	MB_DATA58	Y11	
MA_DATA59	MB_DATA59	AE14	
MA_DATA60	MB_DATA60	AE14	
MA_DATA61	MB_DATA61	AE11	
MA_DATA62	MB_DATA62	AD11	
MA_DATA63	MB_DATA63		

ACPU1C

MEM-DMA

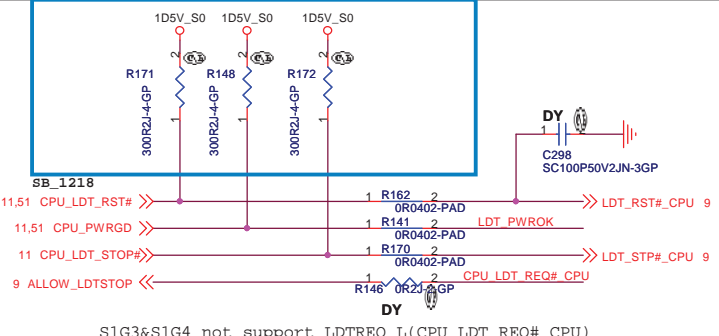
G13	MA_DQS_H0	MB_DQS_H0	C12
H13	MA_DQS_L0	MB_DQS_L0	B12
G16	MA_DQS_H1	MB_DQS_H1	A22
G15	MA_DQS_L1	MB_DQS_L1	E25
C22	MA_DQS_H2	MB_DQS_H2	AE22
C21	MA_DQS_L2	MB_DQS_L2	AE22
G22	MA_DQS_H3	MB_DQS_H3	F26
G21	MA_DQS_L3	MB_DQS_L3	E26
AD23	MA_DQS_H4	MB_DQS_H4	AC25
AC23	MA_DQS_L4	MB_DQS_L4	AC26
AB19	MA_DQS_H5	MB_DQS_H5	AE21
AB20	MA_DQS_L5	MB_DQS_L5	AE22
Y15	MA_DQS_H6	MB_DQS_H6	AE16
W15	MA_DQS_L6	MB_DQS_L6	AD16
W12	MA_DQS_H7	MB_DQS_H7	AE12
W13	MA_DQS_L7	MB_DQS_L7	AE12

SKT-CPU638P,DANUB

JE70-DN

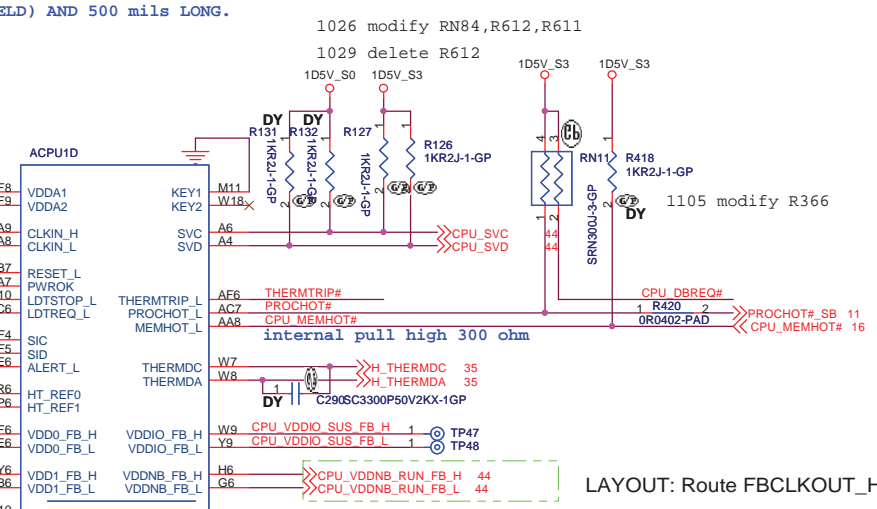
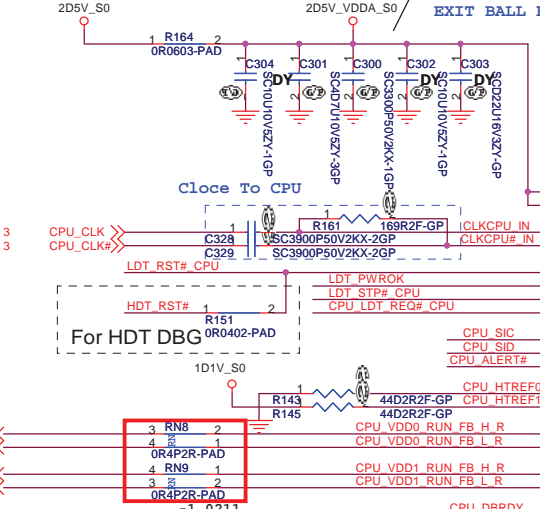
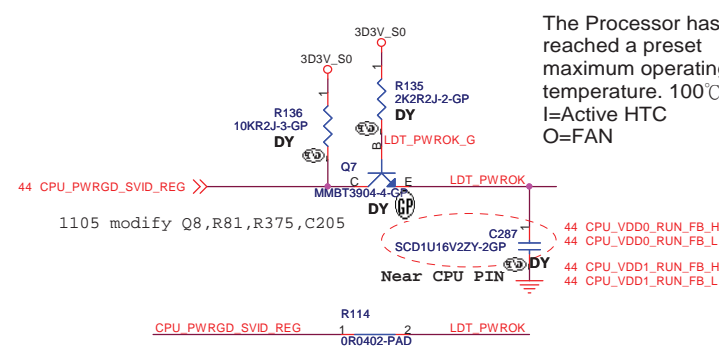
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU DDR (2/4)		
Size			Document Number		
A3			JE70-DN		
Date:			Monday, March 01, 2010		
Sheet			5		
of			63		
Rev			SB		

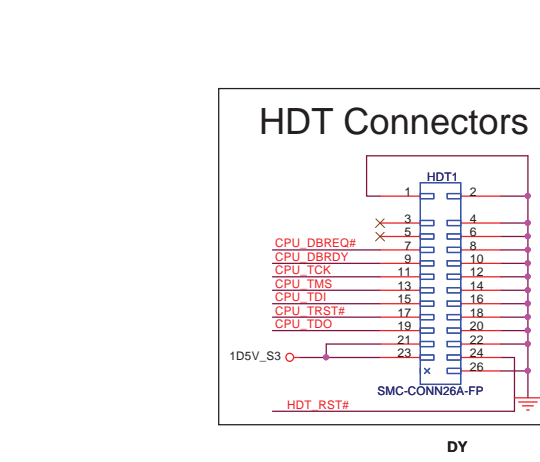
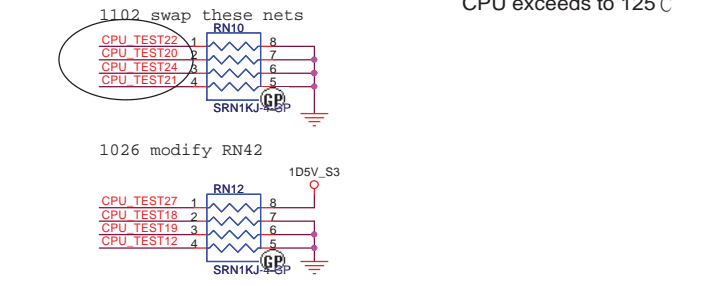
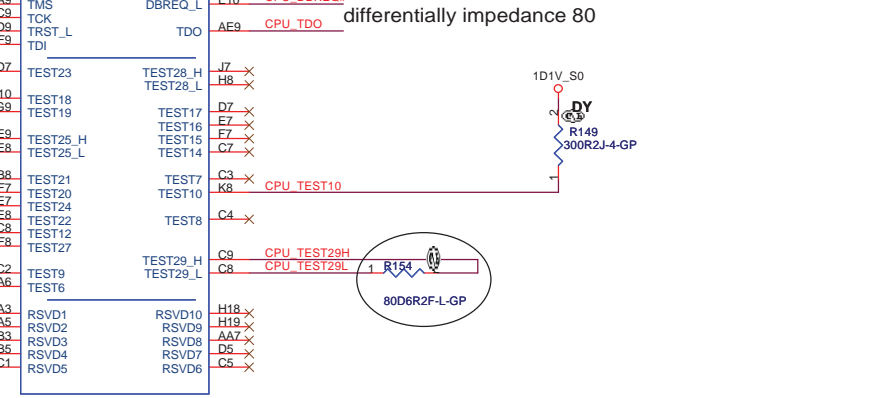
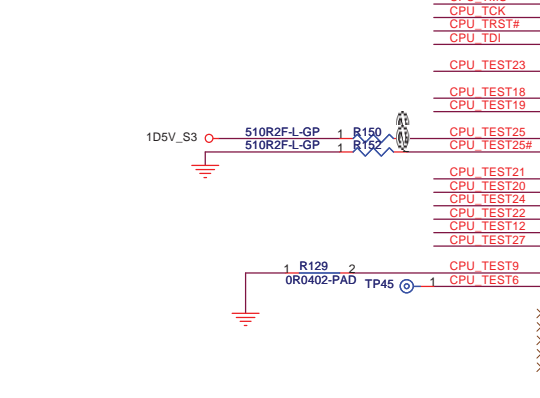
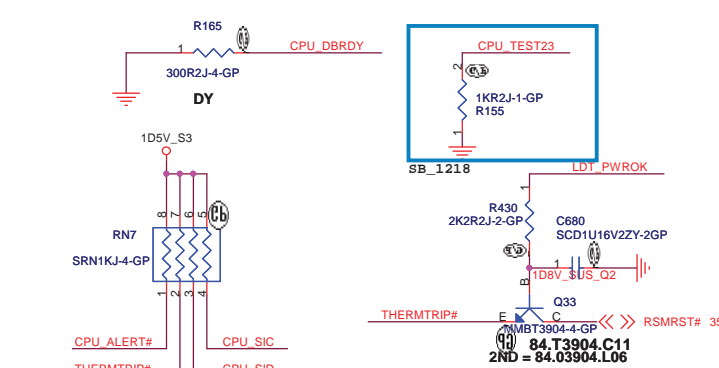


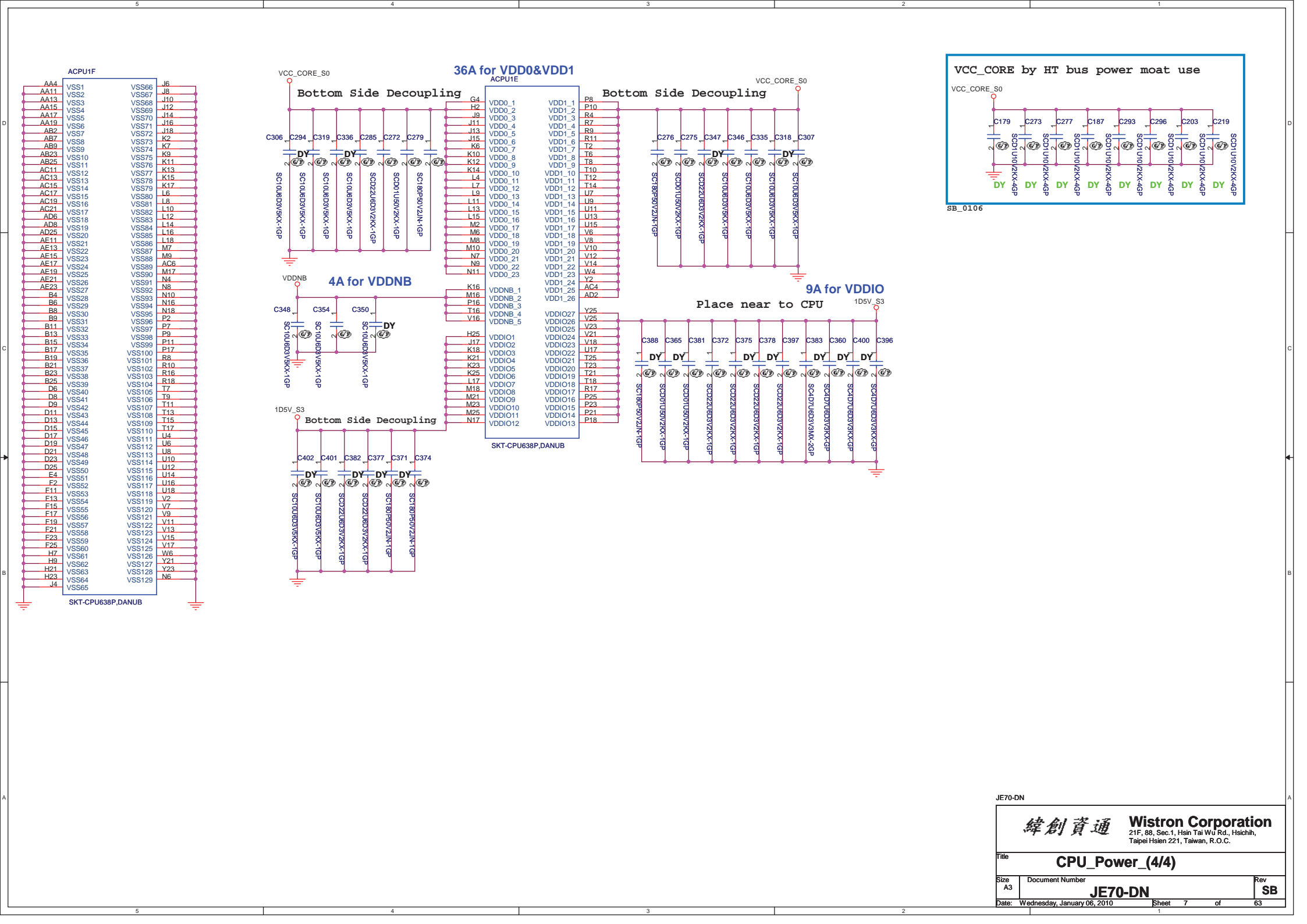
IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

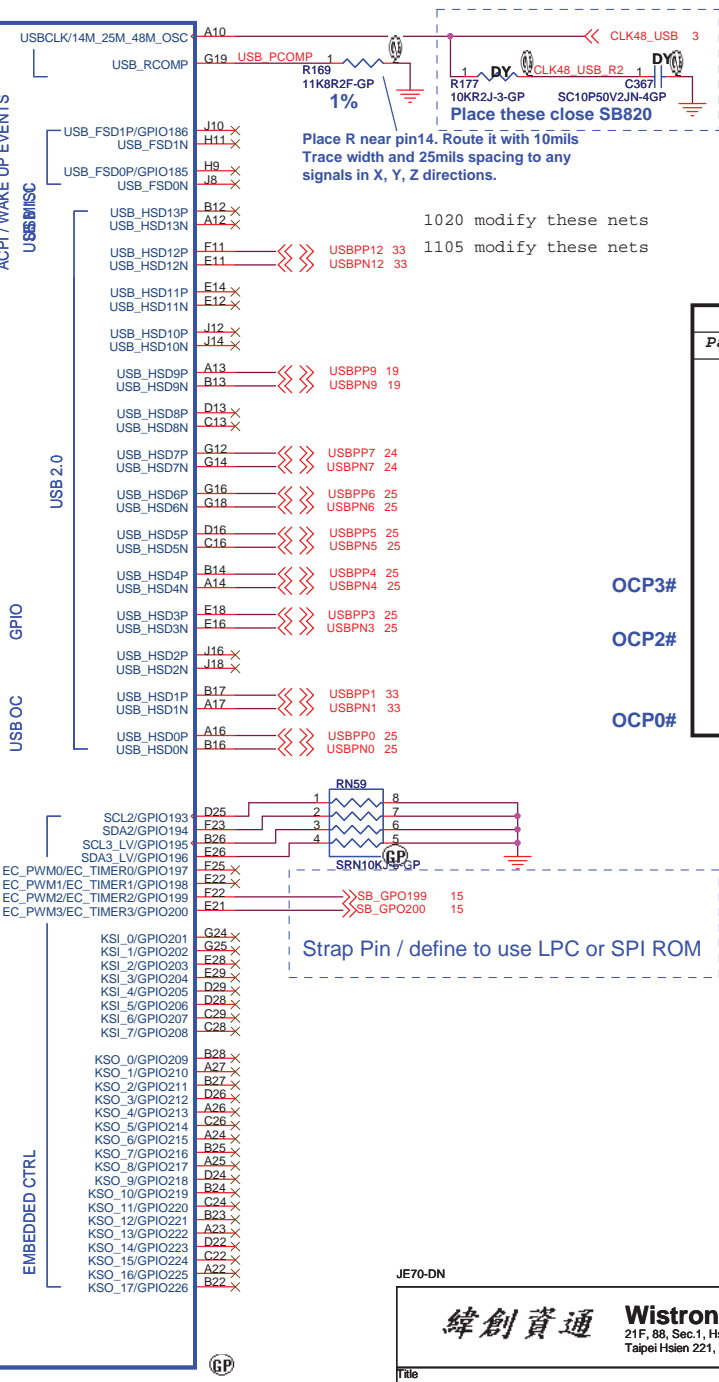
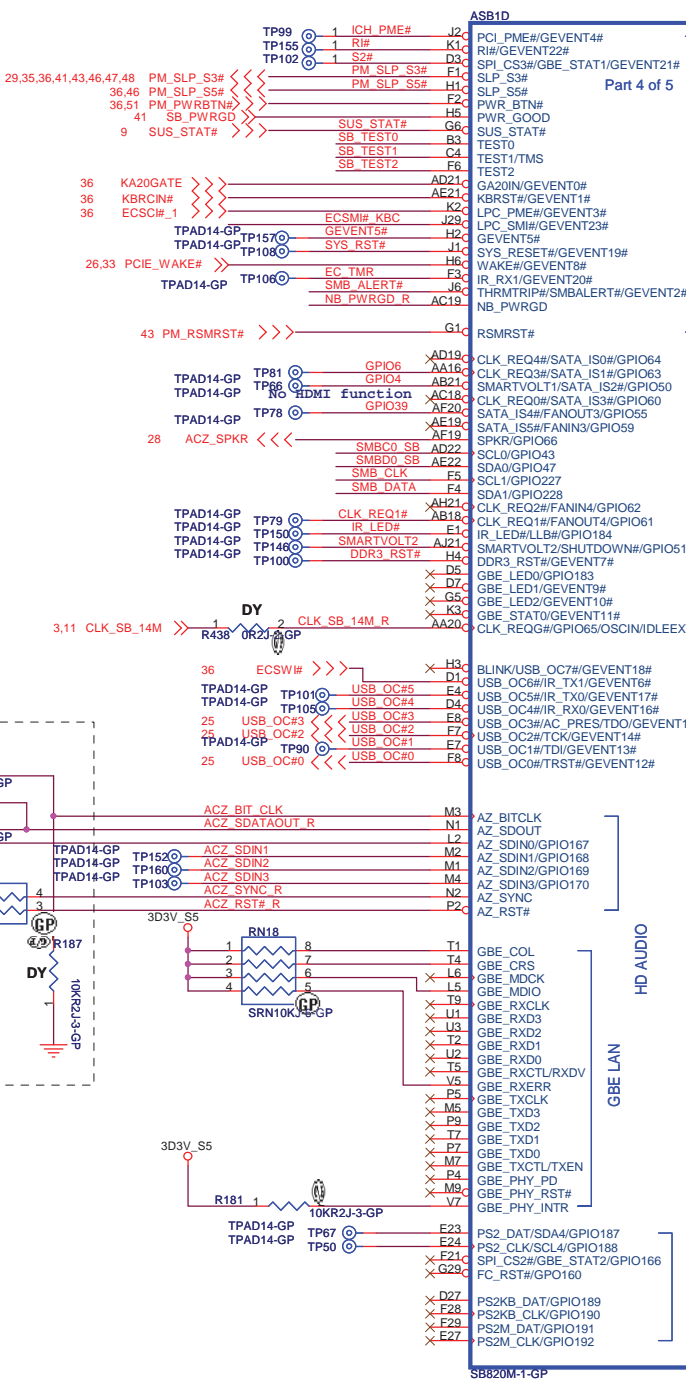
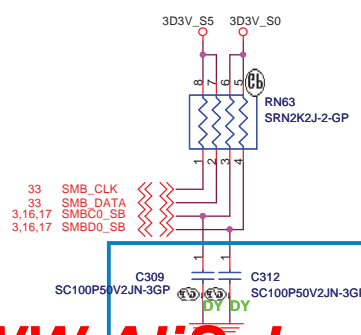


1105 modify Q8,R81,R375,C205
1026 modify R364
1029 delete R364 and add RN127,R946

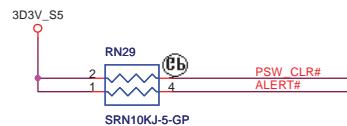
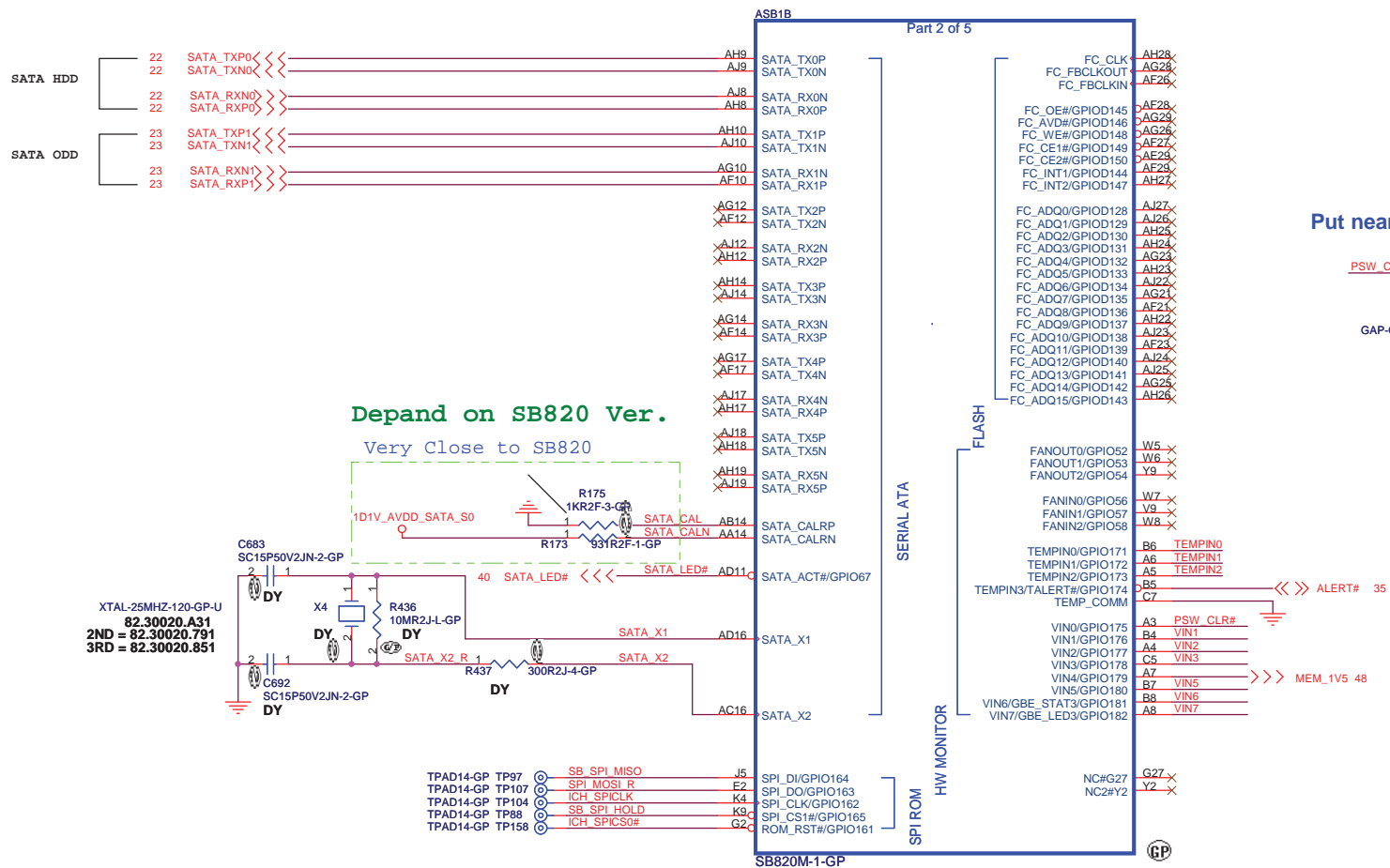








USB	
Pair	Device
12	MINI2 CARD
11	NC
10	NC
9	CCD
8	NC
7	Bluetooth
6	USB3
5	USB2
4	CardReader
3	USB4
2	NC
1	MINI1 CARD
0	USB1



1029 modify the net(SATA_LED#)



JE70-DN

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ATI-SB820 SATA-IDE (3/5)			
Size	Document Number	Rev	SB
A3	JE70-DN		
Date:	Tuesday, February 23, 2010	Sheet	13 of 63

The image displays a detailed PCB layout for the SB820M-1-GP. The layout is organized into several functional areas, each with a specific label and color-coded background:

- POWER (Blue):** This section contains the main power distribution network. It includes labels for various power planes and components, such as **131mA**, **43mA**, **600mA**, **93mA**, **567mA**, **658mA**, and **TBDmA**. The layout also shows the placement of capacitors (e.g., C379, C380, C390, C376, C369, C333, C699, C299, C288, C292, C308, C286, C352, C351, C322, C323, C345, C324, C685, C331, C332, C339, C343, C344, C325, C326, C327, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338, C339, C340, C341, C342, C343, C344, C345, C346, C347, C348, C349, C350, C351, C352, C353, C354, C355, C356, C357, C358, C359, C360, C361, C362, C363, C364, C365, C366, C367, C368, C369, C370, C371, C372, C373, C374, C375, C376, C377, C378, C379, C380, C381, C382, C383, C384, C385, C386, C387, C388, C389, C390, C391, C392, C393, C394, C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411, C412, C413, C414, C415, C416, C417, C418, C419, C420, C421, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C437, C438, C439, C440, C441, C442, C443, C444, C445, C446, C447, C448, C449, C450, C451, C452, C453, C454, C455, C456, C457, C458, C459, C460, C461, C462, C463, C464, C465, C466, C467, C468, C469, C470, C471, C472, C473, C474, C475, C476, C477, C478, C479, C480, C481, C482, C483, C484, C485, C486, C487, C488, C489, C490, C491, C492, C493, C494, C495, C496, C497, C498, C499, C500, C501, C502, C503, C504, C505, C506, C507, C508, C509, C510, C511, C512, C513, C514, C515, C516, C517, C518, C519, C520, C521, C522, C523, C524, C525, C526, C527, C528, C529, C530, C531, C532, C533, C534, C535, C536, C537, C538, C539, C540, C541, C542, C543, C544, C545, C546, C547, C548, C549, C550, C551, C552, C553, C554, C555, C556, C557, C558, C559, C560, C561, C562, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577, C578, C579, C580, C581, C582, C583, C584, C585, C586, C587, C588, C589, C590, C591, C592, C593, C594, C595, C596, C597, C598, C599, C600, C601, C602, C603, C604, C605, C606, C607, C608, C609, C610, C611, C612, C613, C614, C615, C616, C617, C618, C619, C620, C621, C622, C623, C624, C625, C626, C627, C628, C629, C630, C631, C632, C633, C634, C635, C636, C637, C638, C639, C640, C641, C642, C643, C644, C645, C646, C647, C648, C649, C650, C651, C652, C653, C654, C655, C656, C657, C658, C659, C660, C661, C662, C663, C664, C665, C666, C667, C668, C669, C670, C671, C672, C673, C674, C675, C676, C677, C678, C679, C680, C681, C682, C683, C684, C685, C686, C687, C688, C689, C690, C691, C692, C693, C694, C695, C696, C697, C698, C699, C700, C701, C702, C703, C704, C705, C706, C707, C708, C709, C710, C711, C712, C713, C714, C715, C716, C717, C718, C719, C720, C721, C722, C723, C724, C725, C726, C727, C728, C729, C730, C731, C732, C733, C734, C735, C736, C737, C738, C739, C740, C741, C742, C743, C744, C745, C746, C747, C748, C749, C750, C751, C752, C753, C754, C755, C756, C757, C758, C759, C760, C761, C762, C763, C764, C765, C766, C767, C768, C769, C770, C771, C772, C773, C774, C775, C776, C777, C778, C779, C780, C781, C782, C783, C784, C785, C786, C787, C788, C789, C790, C791, C792, C793, C794, C795, C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C808, C809, C810, C811, C812, C813, C814, C815, C816, C817, C818, C819, C820, C821, C822, C823, C824, C825, C826, C827, C828, C829, C830, C831, C832, C833, C834, C835, C836, C837, C838, C839, C840, C841, C842, C843, C844, C845, C846, C847, C848, C849, C850, C851, C852, C853, C854, C855, C856, C857, C858, C859, C860, C861, C862, C863, C864, C865, C866, C867, C868, C869, C870, C871, C872, C873, C874, C875, C876, C877, C878, C879, C880, C881, C882, C883, C884, C885, C886, C887, C888, C889, C890, C891, C892, C893, C894, C895, C896, C897, C898, C899, C900, C901, C902, C903, C904, C905, C906, C907, C908, C909, C910, C911, C912, C913, C914, C915, C916, C917, C918, C919, C920, C921, C922, C923, C924, C925, C926, C927, C928, C929, C930, C931, C932, C933, C934, C935, C936, C937, C938, C939, C940, C941, C942, C943, C944, C945, C946, C947, C948, C949, C950, C951, C952, C953, C954, C955, C956, C957, C958, C959, C960, C961, C962, C963, C964, C965, C966, C967, C968, C969, C970, C971, C972, C973, C974, C975, C976, C977, C978, C979, C980, C981, C982, C983, C984, C985, C986, C987, C988, C989, C990, C991, C992, C993, C994, C995, C996, C997, C998, C999, C1000, C1001, C1002, C1003, C1004, C1005, C1006, C1007, C1008, C1009, C1010, C1011, C1012, C1013, C1014, C1015, C1016, C1017, C1018, C1019, C1020, C1021, C1022, C1023, C1024, C1025, C1026, C1027, C1028, C1029, C1030, C1031, C1032, C1033, C1034, C1035, C1036, C1037, C1038, C1039, C1040, C1041, C1042, C1043, C1044, C1045, C1046, C1047, C1048, C1049, C1050, C1051, C1052, C1053, C1054, C1055, C1056, C1057, C1058, C1059, C1060, C1061, C1062, C1063, C1064, C1065, C1066, C1067, C1068,

ASB1E

Part 5 of 5

Y14	VSSIO, SATA	V5S	A12
Y16	VSSIO, SATA	V5S	A28
AB1A	VSSIO, SATA	V5S	E5
AC1A	VSSIO, SATA	V5S	D23
AE1A	VSSIO, SATA	V5S	E28
AF1A	VSSIO, SATA	V5S	E6
AF1B	VSSIO, SATA	V5S	F24
AF1C	VSSIO, SATA	V5S	H15
AG1A	VSSIO, SATA	V5S	R13
AH1A	VSSIO, SATA	V5S	R17
AH1B	VSSIO, SATA	V5S	T10
AH1C	VSSIO, SATA	V5S	T10
AH1D	VSSIO, SATA	V5S	T10
AH1E	VSSIO, SATA	V5S	T10
AJ11	VSSIO, SATA	V5S	M18
AJ12	VSSIO, SATA	V5S	M18
AJ13	VSSIO, SATA	V5S	M18
AJ16	VSSIO, SATA	V5S	M18
AJ17	VSSIO, SATA	V5S	M18
AJ18	VSSIO, SATA	V5S	M18
AJ19	VSSIO, SATA	V5S	M18
AJ20	VSSIO, SATA	V5S	M18
AJ21	VSSIO, SATA	V5S	M18
AJ22	VSSIO, SATA	V5S	M18
AJ23	VSSIO, SATA	V5S	M18
AJ24	VSSIO, SATA	V5S	M18
AJ25	VSSIO, SATA	V5S	M18
AJ26	VSSIO, SATA	V5S	M18
AJ27	VSSIO, SATA	V5S	M18
AJ28	VSSIO, SATA	V5S	M18
AJ29	VSSIO, SATA	V5S	M18
AJ30	VSSIO, SATA	V5S	M18
AJ31	VSSIO, SATA	V5S	M18
AJ32	VSSIO, SATA	V5S	M18
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AJ34	VSSIO, SATA	V5S	M18
AJ35	VSSIO, SATA	V5S	M18
AJ36	VSSIO, SATA	V5S	M18
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AJ42	VSSIO, SATA	V5S	M18
AJ43	VSSIO, SATA	V5S	M18
AJ44	VSSIO, SATA	V5S	M18
AJ45	VSSIO, SATA	V5S	M18
AJ46	VSSIO, SATA	V5S	M18
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AJ51	VSSIO, SATA	V5S	M18
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AJ54	VSSIO, SATA	V5S	M18
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AJ56	VSSIO, SATA	V5S	M18
AJ57	VSSIO, SATA	V5S	M18
AJ58	VSSIO, SATA	V5S	M18
AJ59	VSSIO, SATA	V5S	M18
AJ60	VSSIO, SATA	V5S	M18
AJ61	VSSIO, SATA	V5S	M18
AJ62	VSSIO, SATA	V5S	M18
AJ63	VSSIO, SATA	V5S	M18
AJ64	VSSIO, SATA	V5S	M18
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AJ71	VSSIO, SATA	V5S	M18
AJ72	VSSIO, SATA	V5S	M18
AJ73	VSSIO, SATA	V5S	M18
AJ74	VSSIO, SATA	V5S	M18
AJ75	VSSIO, SATA	V5S	M18
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AJ77	VSSIO, SATA	V5S	M18
AJ78	VSSIO, SATA	V5S	M18
AJ79	VSSIO, SATA	V5S	M18
AJ80	VSSIO, SATA	V5S	M18
AJ81	VSSIO, SATA	V5S	M18
AJ82	VSSIO, SATA	V5S	M18
AJ83	VSSIO, SATA	V5S	M18
AJ84	VSSIO, SATA	V5S	M18
AJ85	VSSIO, SATA	V5S	M18
AJ86	VSSIO, SATA	V5S	M18
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AJ89	VSSIO, SATA	V5S	M18
AJ90	VSSIO, SATA	V5S	M18
AJ91	VSSIO, SATA	V5S	M18
AJ92	VSSIO, SATA	V5S	M18
AJ93	VSSIO, SATA	V5S	M18
AJ94	VSSIO, SATA	V5S	M18
AJ95	VSSIO, SATA	V5S	M18
AJ96	VSSIO, SATA	V5S	M18
AJ97	VSSIO, SATA	V5S	M18
AJ98	VSSIO, SATA	V5S	M18
AJ99	VSSIO, SATA	V5S	M18
AJ100	VSSIO, SATA	V5S	M18
AJ101	VSSIO, SATA	V5S	M18
AJ102	VSSIO, SATA	V5S	M18
AJ103	VSSIO, SATA	V5S	M18
AJ104	VSSIO, SATA	V5S	M18
AJ105	VSSIO, SATA	V5S	M18

Y4	EFUSE	V5S	L8
M19	VSSXL	V5SPL_SYS	M20
D8	VSSAN_HWM		A2

P21	VSSIO, PCIeCLK	VSSIO, PCIeCLK	H23
P20	VSSIO, PCIeCLK	VSSIO, PCIeCLK	H28
M2	VSSIO, PCIeCLK	VSSIO, PCIeCLK	AA21
M24	VSSIO, PCIeCLK	VSSIO, PCIeCLK	AA23
P22	VSSIO, PCIeCLK	VSSIO, PCIeCLK	AA25
P24	VSSIO, PCIeCLK	VSSIO, PCIeCLK	AD23
P26	VSSIO, PCIeCLK	VSSIO, PCIeCLK	AA26
P28	VSSIO, PCIeCLK	VSSIO, PCIeCLK	AC26
T20	VSSIO, PCIeCLK	VSSIO, PCIeCLK	T20
T22	VSSIO, PCIeCLK	VSSIO, PCIeCLK	W21
T24	VSSIO, PCIeCLK	VSSIO, PCIeCLK	W20
T26	VSSIO, PCIeCLK	VSSIO, PCIeCLK	AE26
J23	VSSIO, PCIeCLK	VSSIO, PCIeCLK	L21
J20	VSSIO, PCIeCLK	VSSIO, PCIeCLK	K20

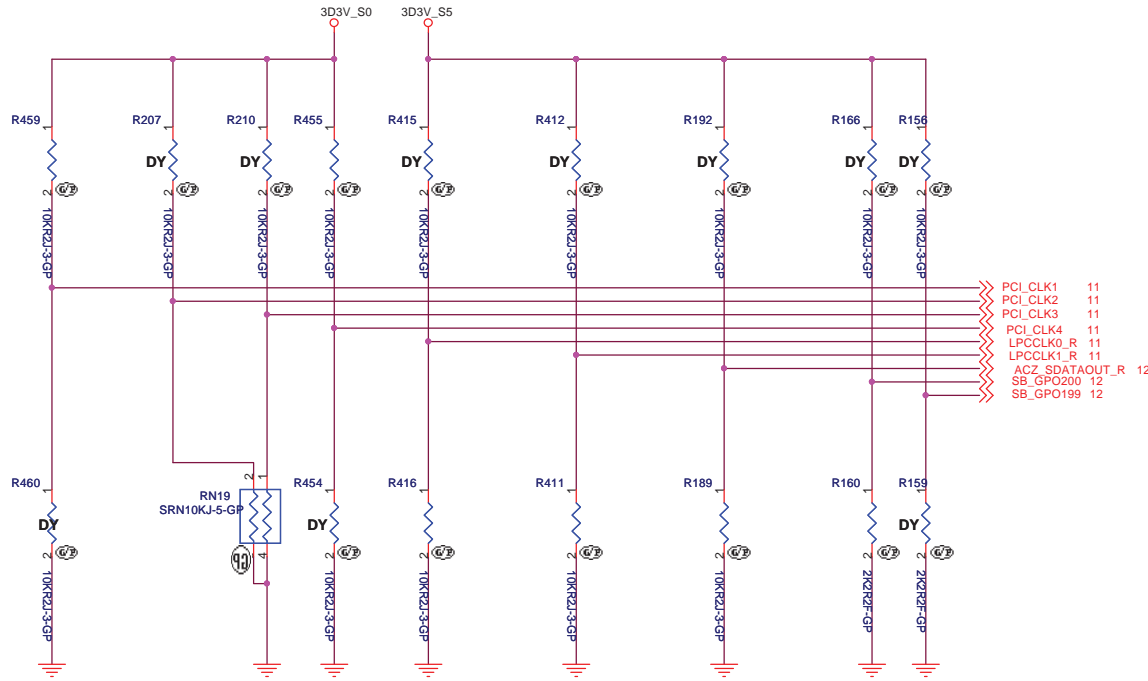
98870M-1-EP

GP

 緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ATI-SB820 POWER&GND (4/5)			
Size	Document Number		Rev
Custom	JE70-DN		SE
Date:	Friday, February 12, 2010	Sheet 14 of	63

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



1118 modify R412,R411

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200	GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	LOW POWER MODE	H,H = Reserved H,L = SPI ROM	
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	

NOTE: SB820 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS

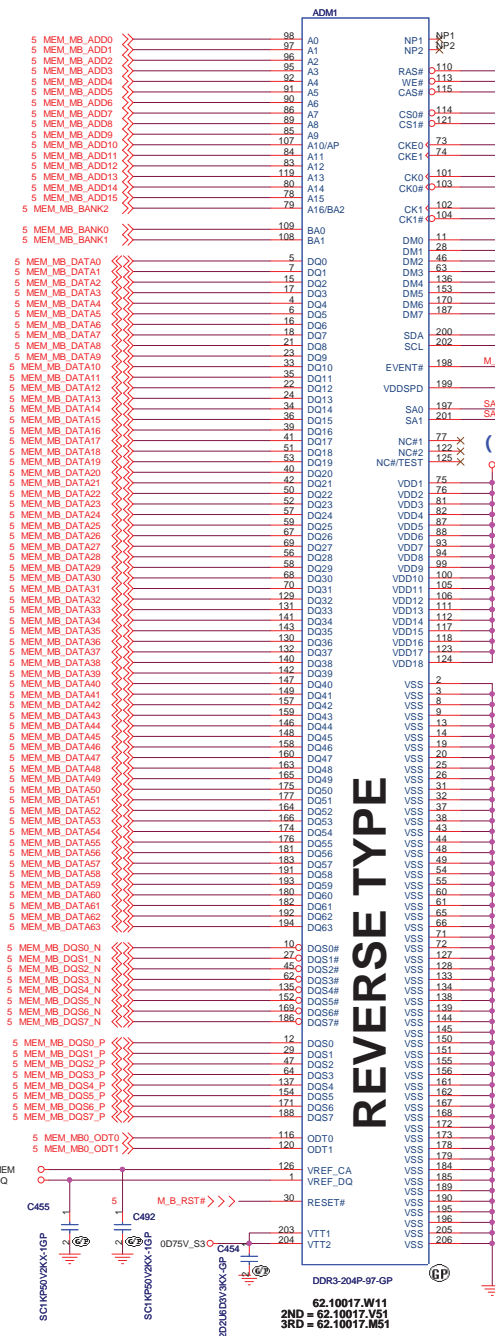
TPAD14-GP	TP89	PCI_AD23	11
TPAD14-GP	TP87	PCI_AD24	11
TPAD14-GP	TP85	PCI_AD25	11
TPAD14-GP	TP93	PCI_AD26	11
TPAD14-GP	TP98	PCI_AD27	11
TPAD14-GP	TP156	PCI_AD28	11
TPAD14-GP	TP159	PCI_AD29	11
TPAD14-GP	TP154	PCI_AD30	11

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

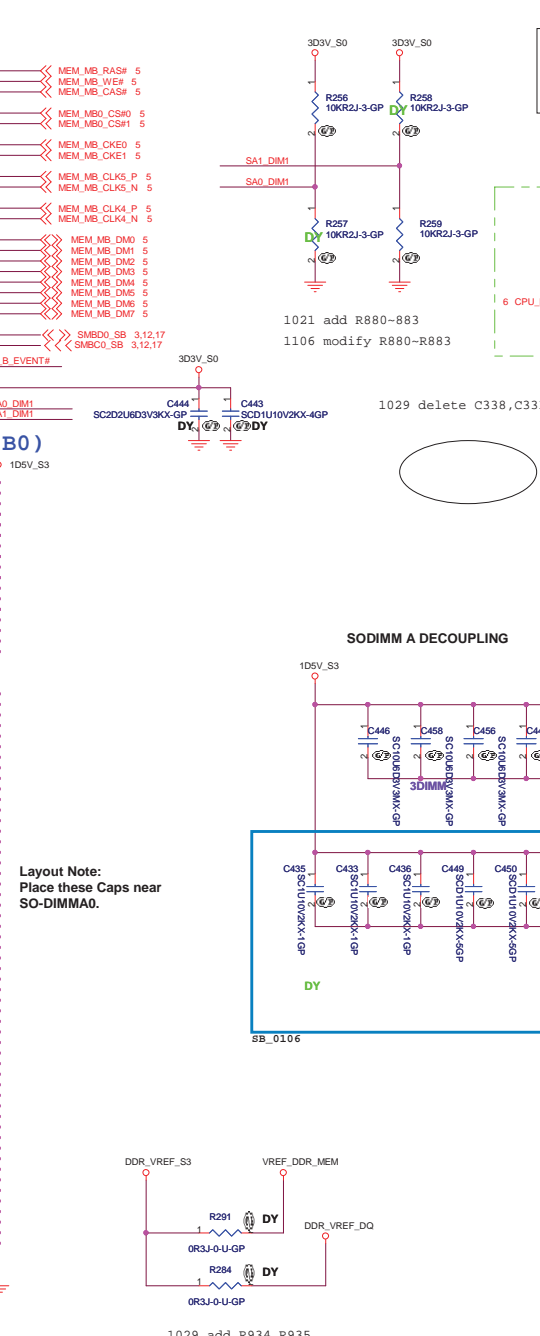
JE70-DN

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
ATI-SB820 STRAPPING (5/5)	
Size	Document Number
A3	JE70-DN
Date: Tuesday, February 23, 2010	Rev SB
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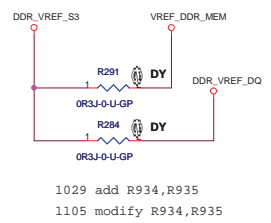


REVERSE TYPE

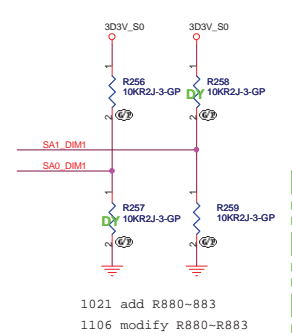
62.10017.W11
2ND = 62.10017.V51
3RD = 62.10017.M51
1106 modify ADM1



Layout Note:
Place these Caps near
SO-DIMMA0.



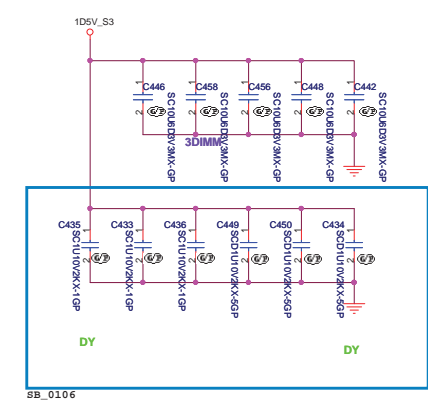
1029 add R934,R935
1105 modify R934,R935



1021 add R880-883
1106 modify R880-R883

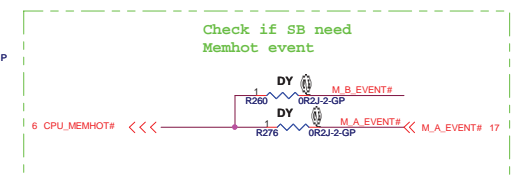
1029 delete C338,C331

SODIMM A DECOUPLING



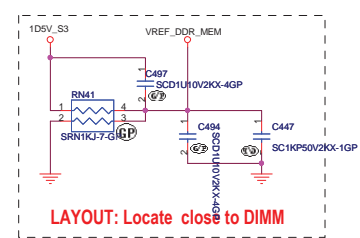
SB_0106

Note:
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is
SO-DIMMA TS Address is



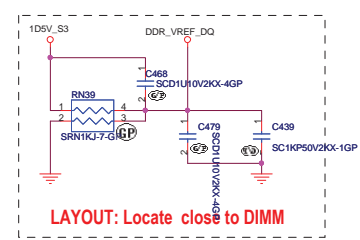
Check if SB need
Memhot event

VREF_DDR_MEM

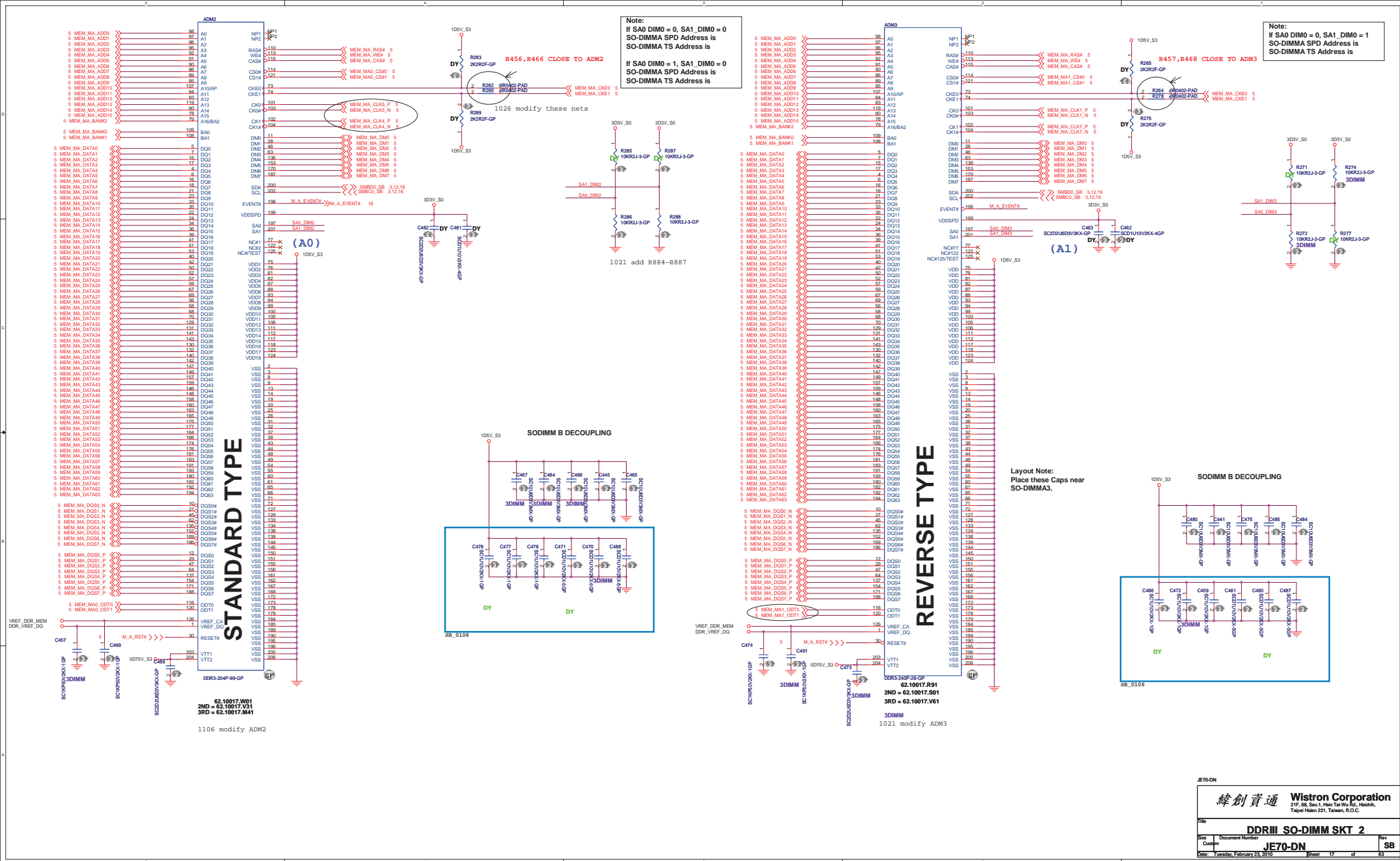


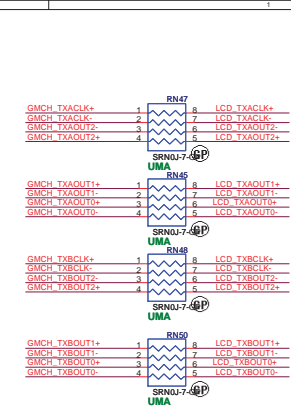
LAYOUT: Locate close to DIMM

DDR_VREF_DQ



LAYOUT: Locate close to DIMM





SRN0J-7-G-6P

UMA

9 GMCH_RED >>> 1 8 >>> CRT_RED 20
 9 GMCH_GREEN >>> 2 7 >>> CRT_GREEN 20
 9 GMCH_BLUE >>> 3 6 >>> CRT_BLUE 20

SRN0J-7-G-6P

UMA

9 DAT_DOC_EDID >>> 1 8 >>> LCD_EDID_DAT_1 19
 9 CLK_DOC_EDID >>> 2 7 >>> LCD_EDID_CLK_1 19

SRN0J-7-G-6P

DIS_only

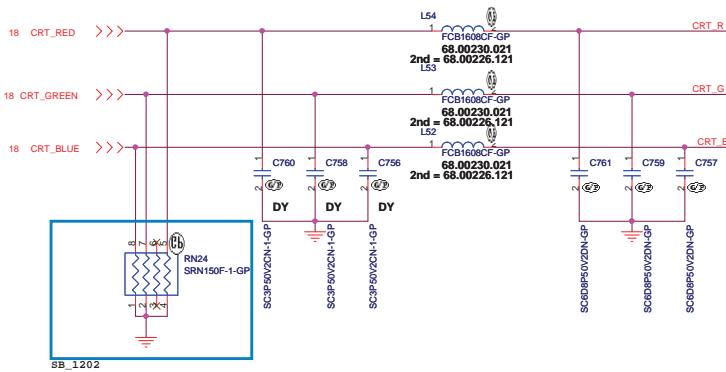
53 MA_CRT_BLUE >>> 1 8 >>> CRT_BLUE 20
 53 MA_CRT_GREEN >>> 2 7 >>> CRT_GREEN 20
 53 MA_CRT_RED >>> 3 6 >>> CRT_RED 20

[illegible]

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

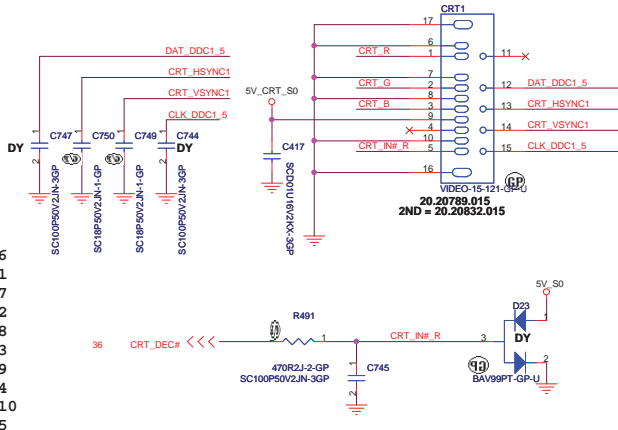
Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 10 ohm@100MHz



Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

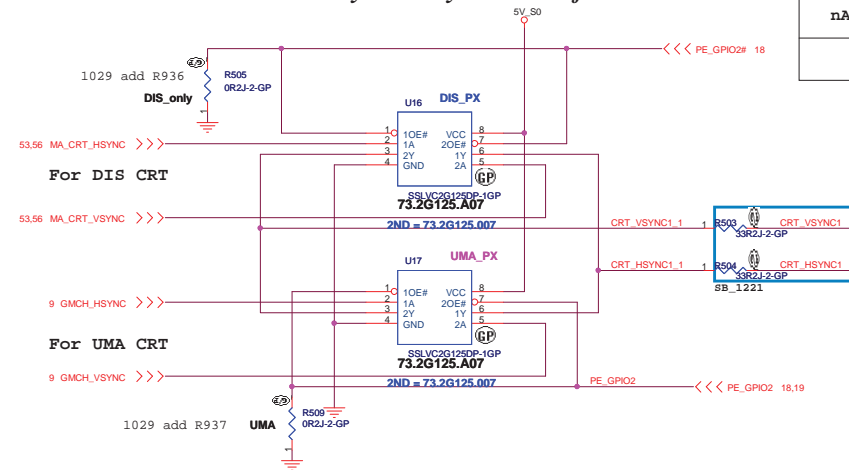
CRT I/F & CONNECTOR



Hsync & Vsync level shift

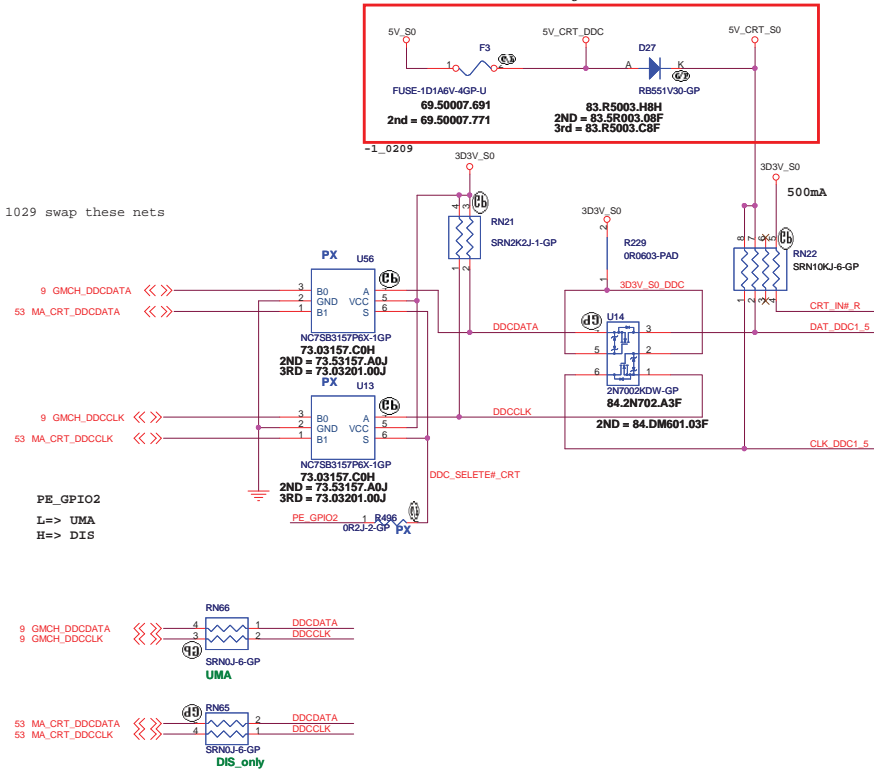
Function	OE#
nA to nY	L
X	H

PE_GPIO2
L=> UMA
H=> DIS



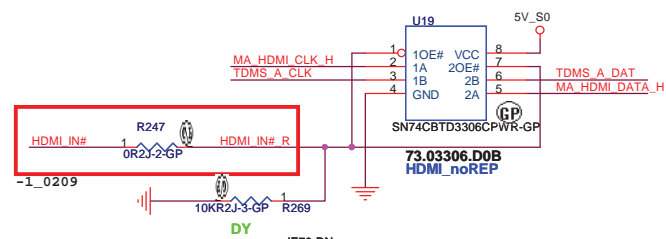
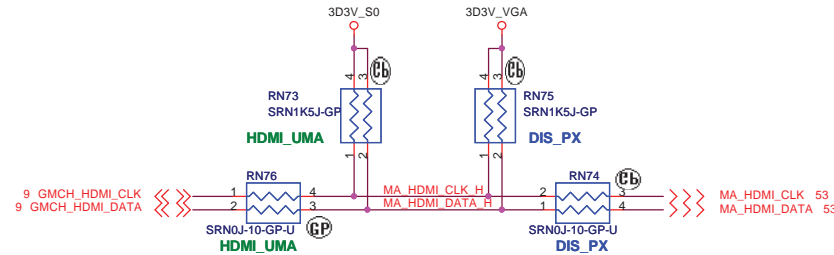
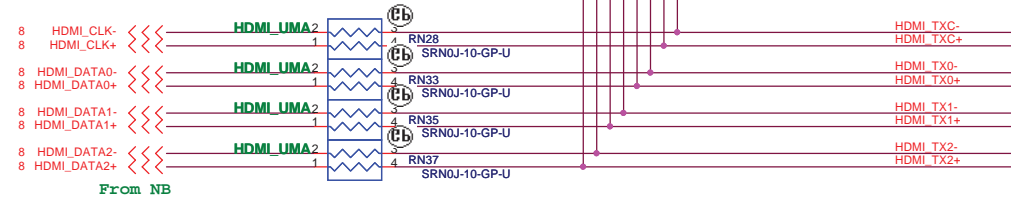
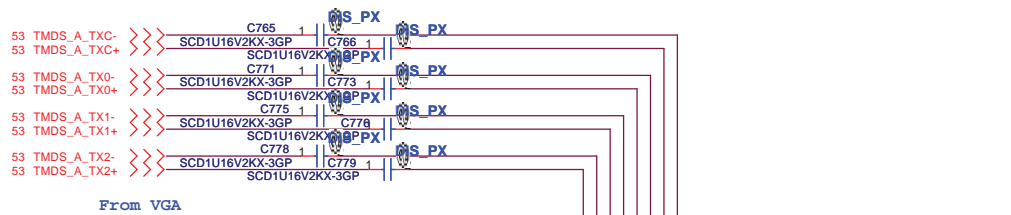
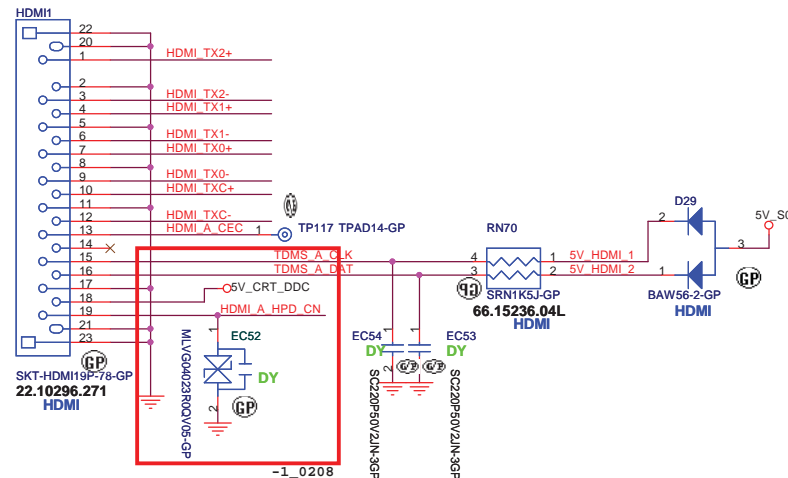
DDC_CLK & DATA level shift

1029 swap these nets

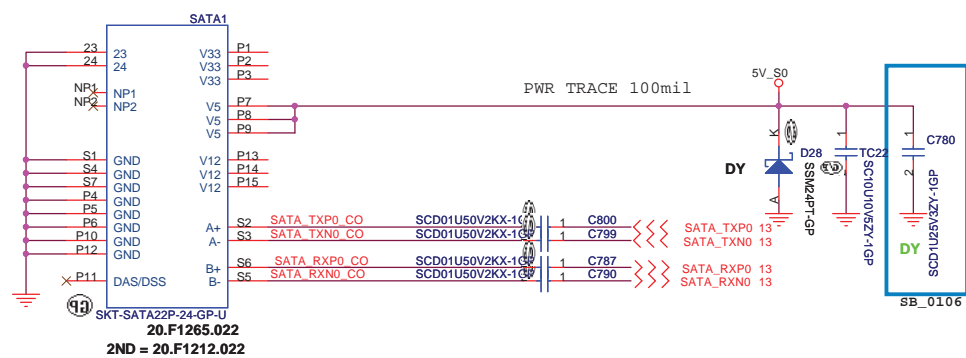


JE70-DN

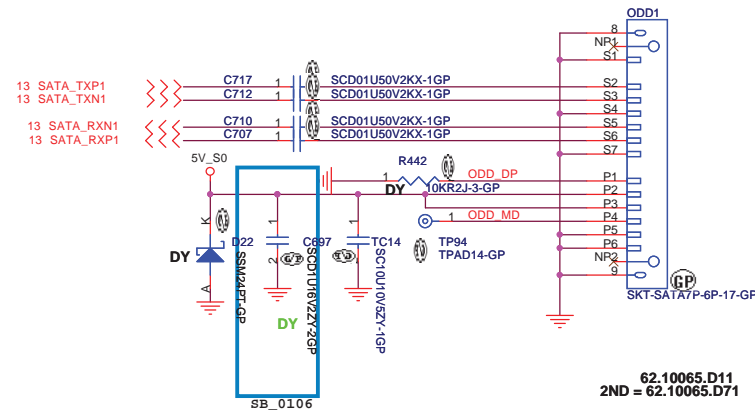
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Size	
Document Number	
Date	
Sheet	
of	
Rev	
SB	



SATA Connector



ODD Connector



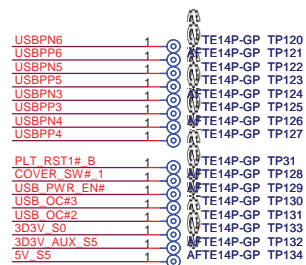
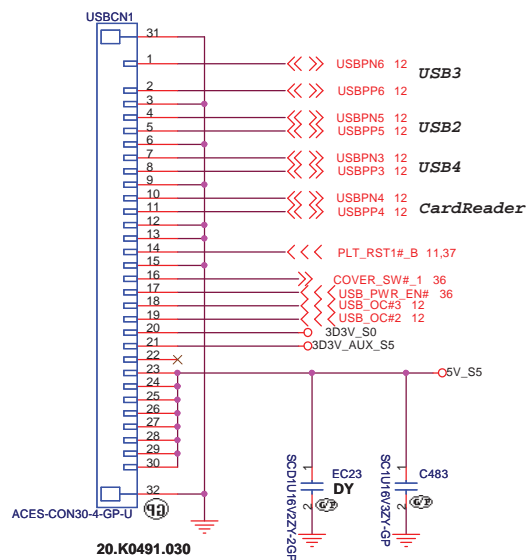
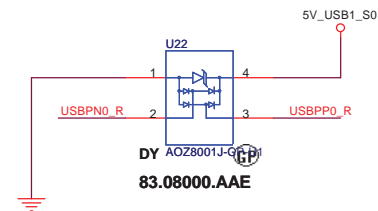
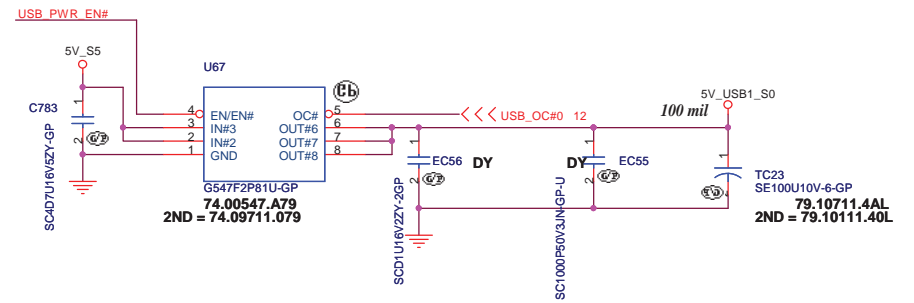
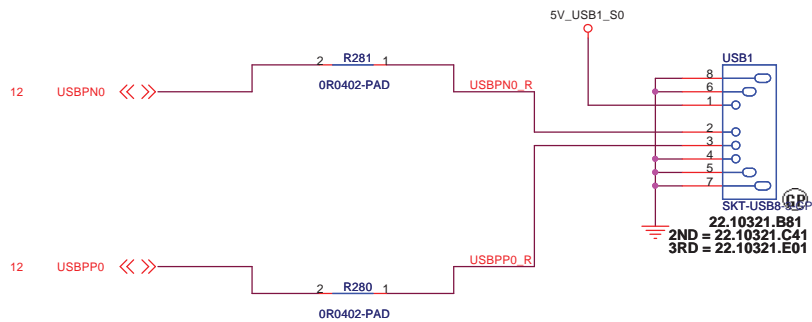
JE70-DN

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ODD			
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1.5A / High Active Voltage 2V

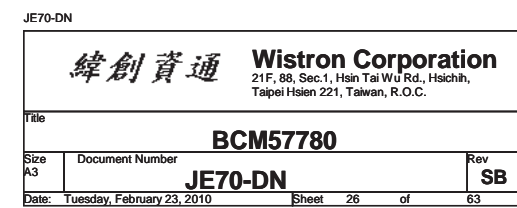


Title			
BLUETOOTH			
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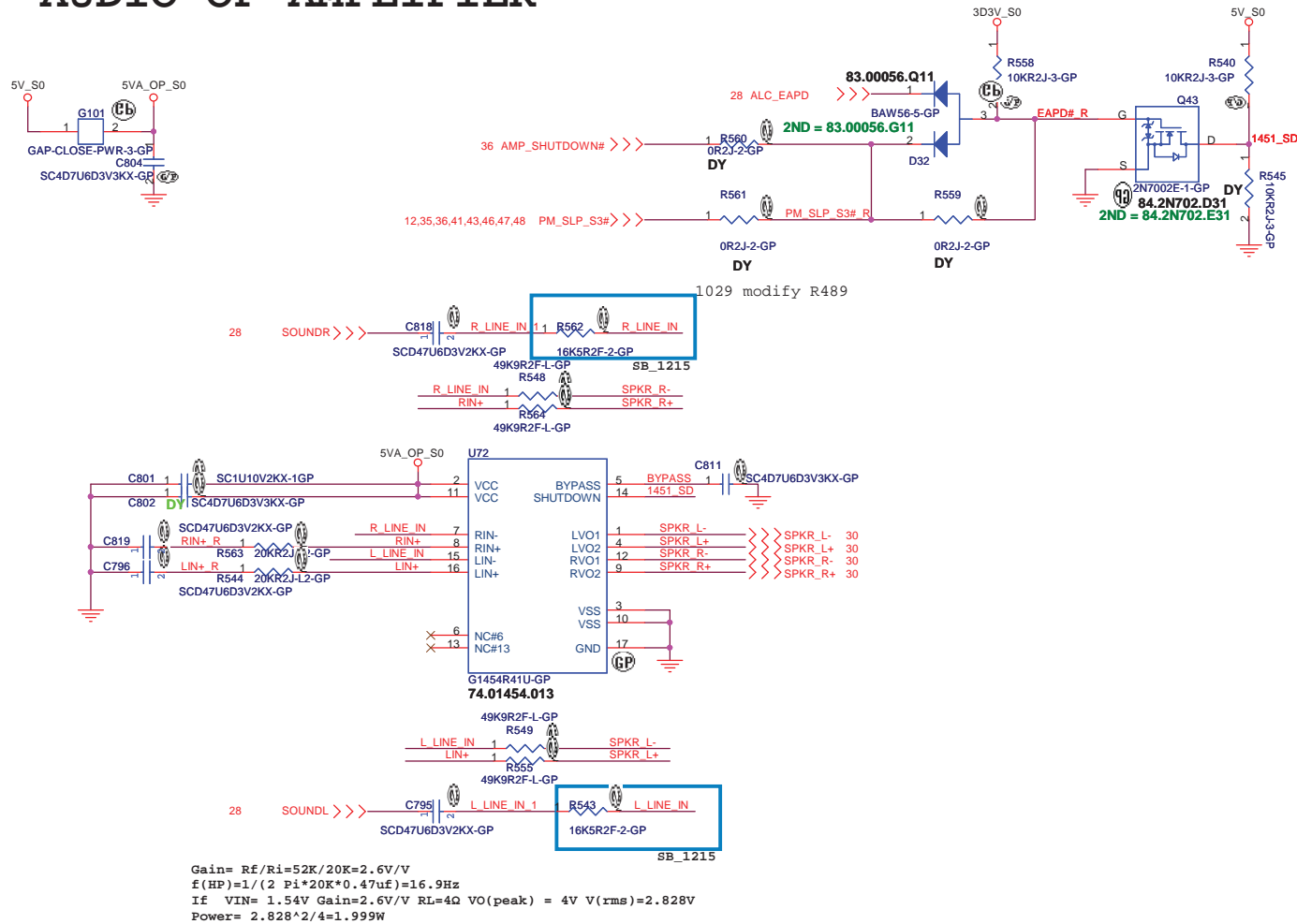


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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB			
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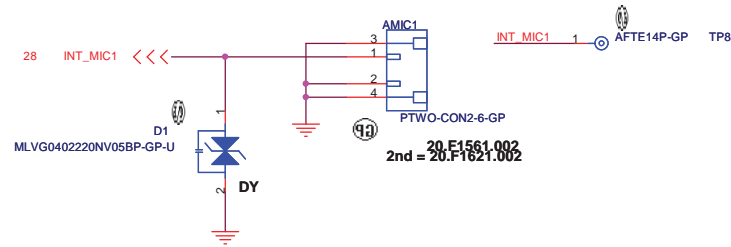
AUDIO OP AMPLIFIER



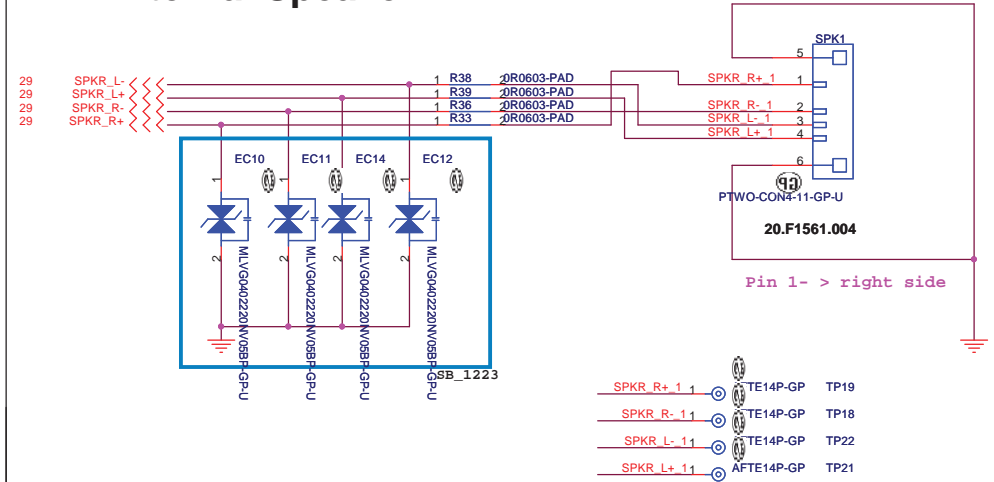
JE70-DN

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AUDIO AMP			
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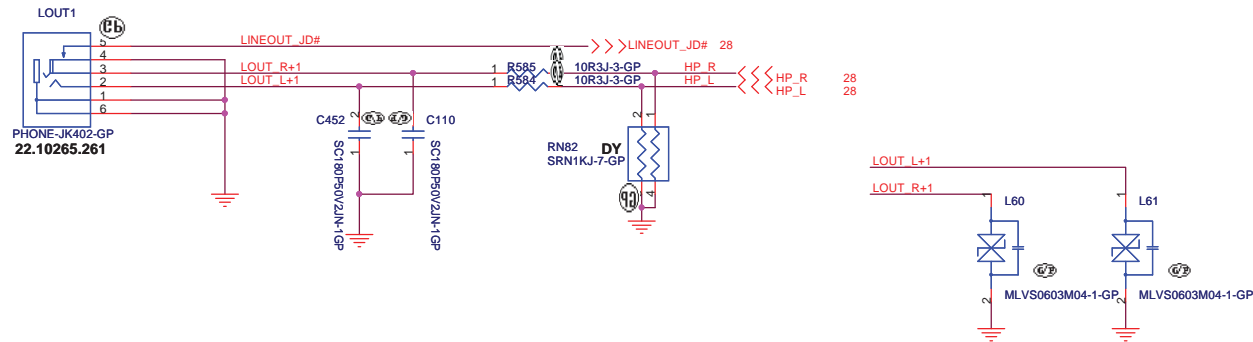
Internal Mic



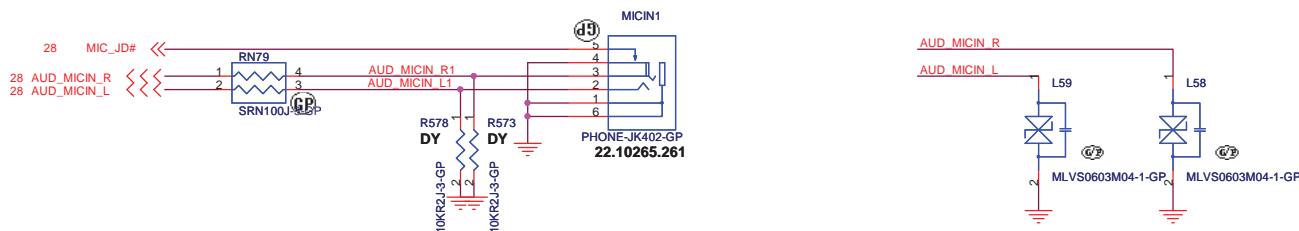
Internal Speaker



LINE OUT



MIC IN



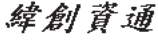
JE70-DN

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Taipei Hsien 221, Taiwan, R.O.C.

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AUDIO JACK			SB
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No Modem Function

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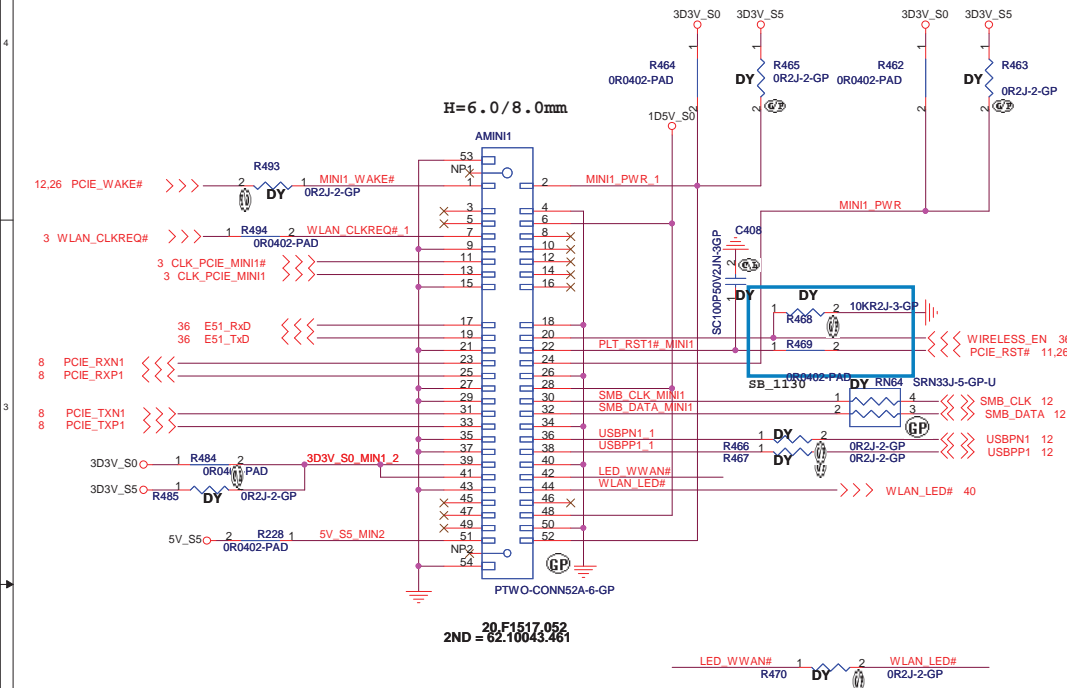
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MDC			
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5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD) on USB board

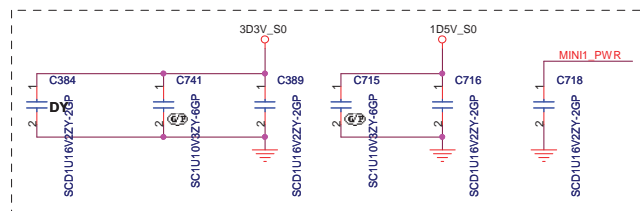
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緯創資通		Wistron Corporation	
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Title			
CARDREADER			
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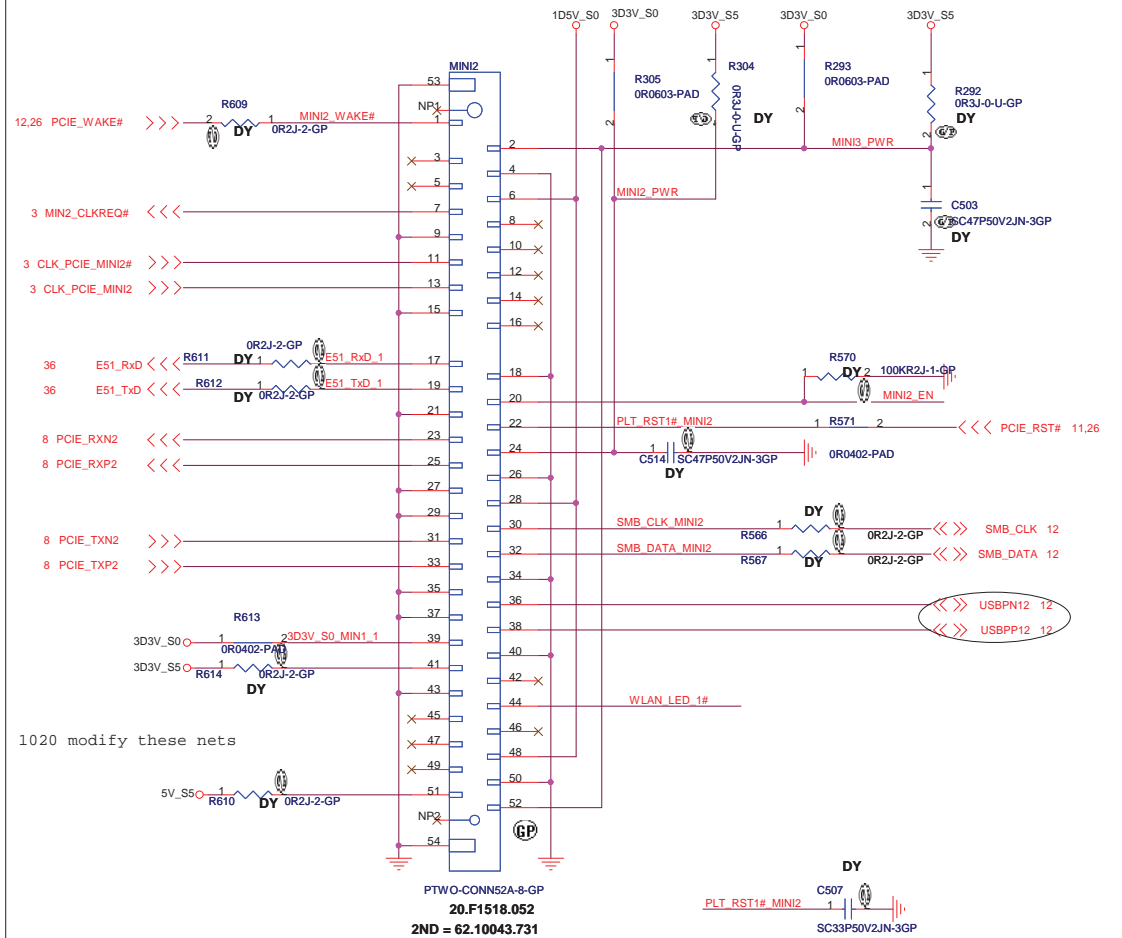
Mini Card Connector(WLAN)



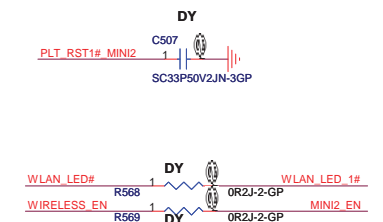
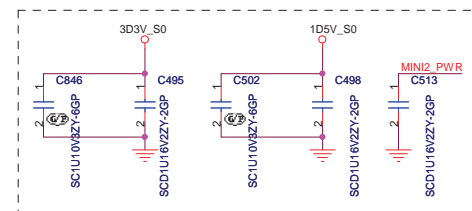
Place near AMIN11



Mini Card Function



Place near MINIC2



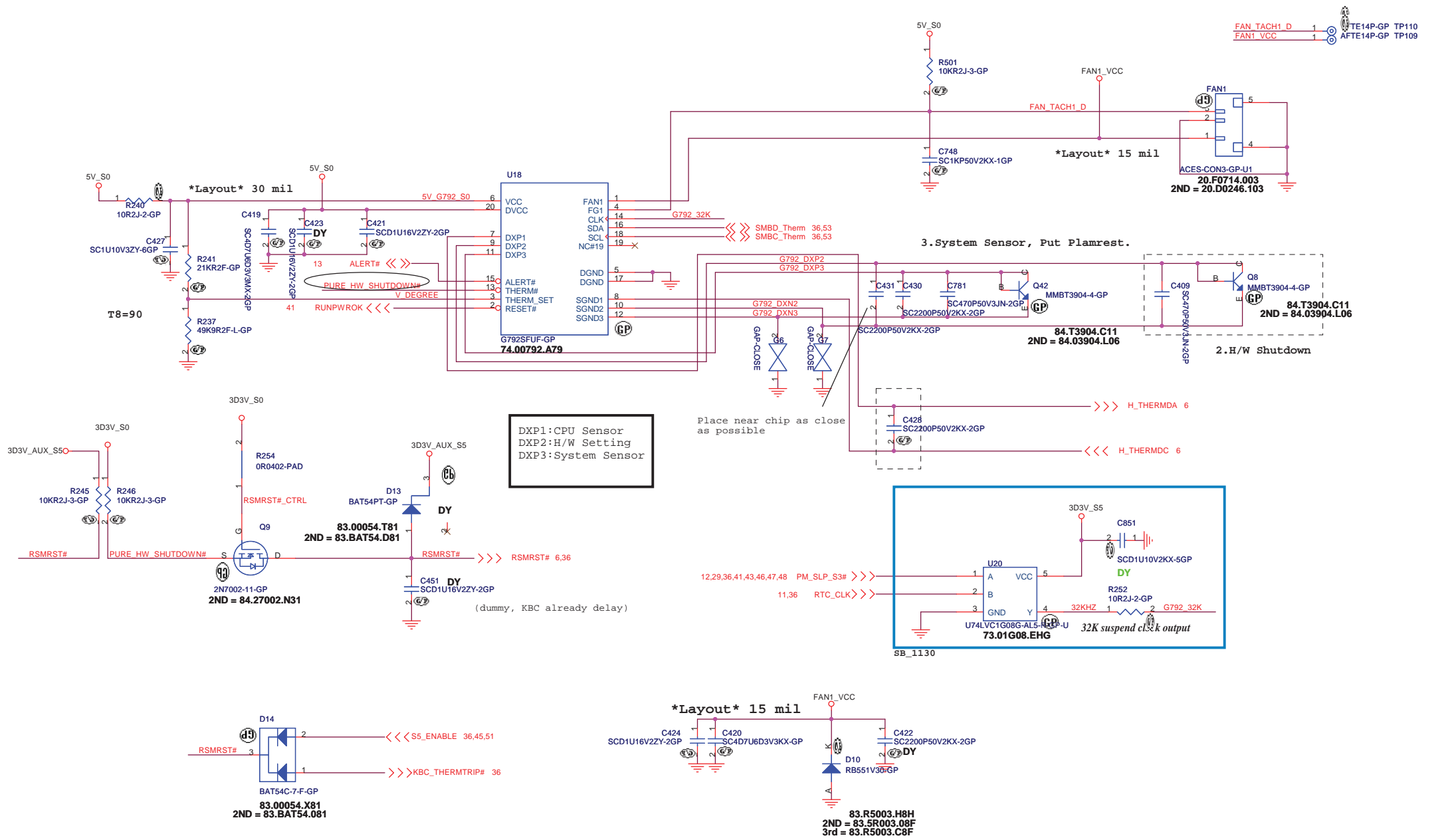
JE70-DN

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
MINI CARD		
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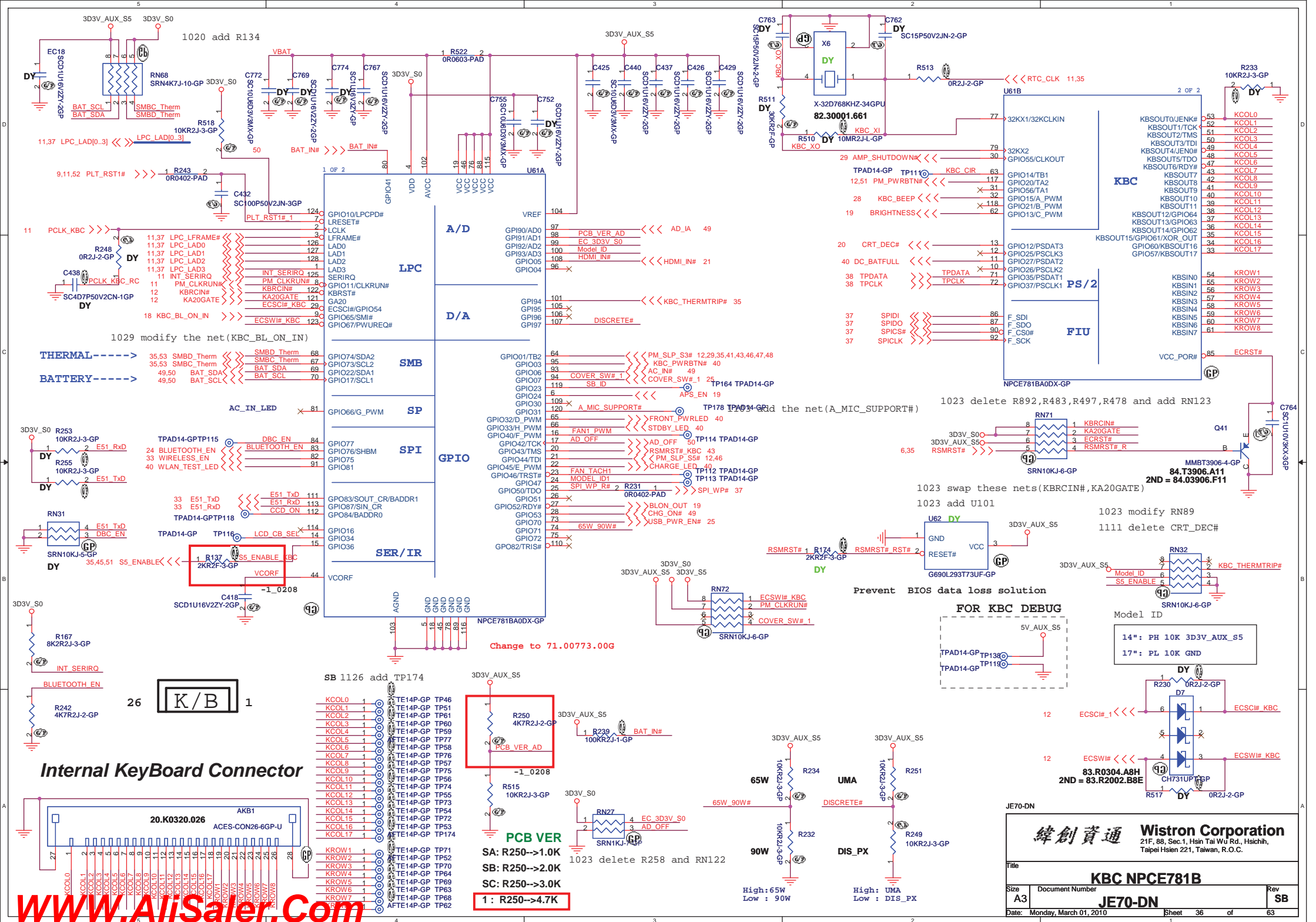
No NEWCARD Function

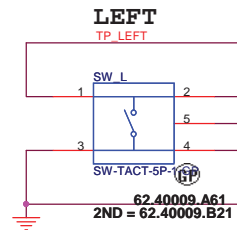
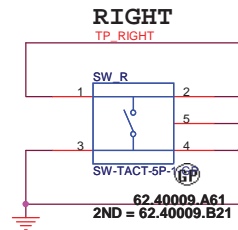
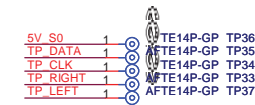
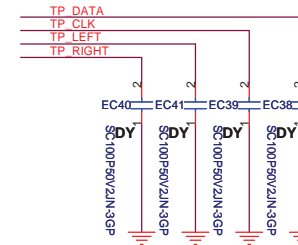
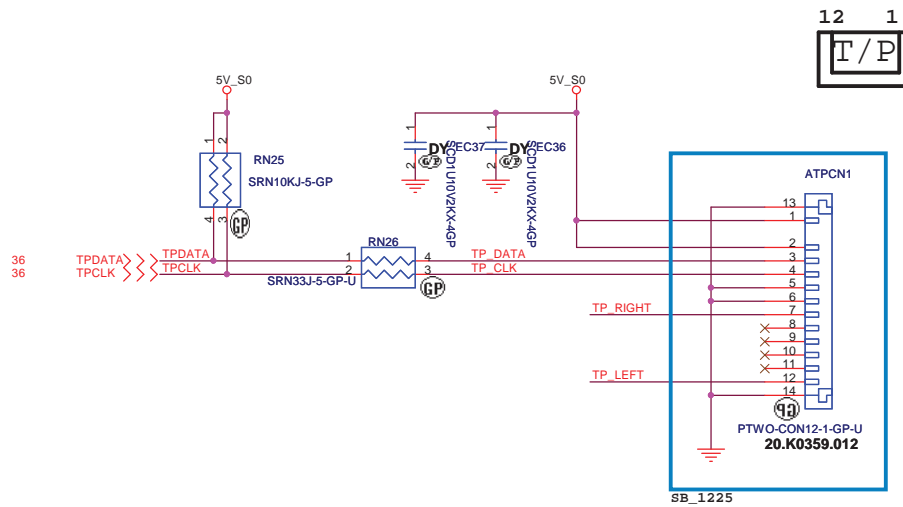
JE70-DN

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NEW CARD			
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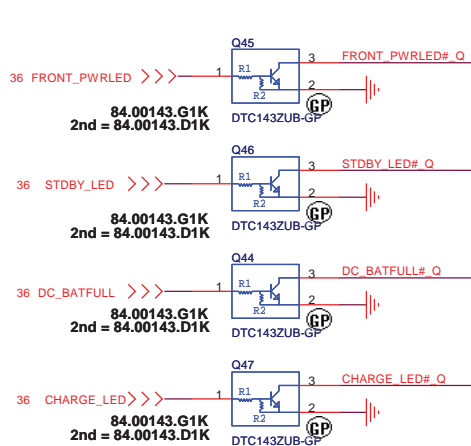
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Title		Touch PAD	
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NONE BOARD

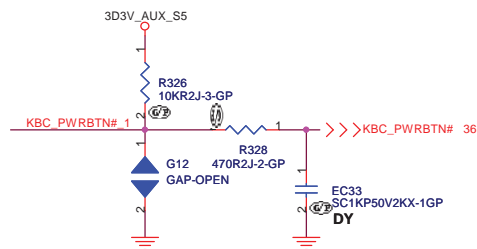
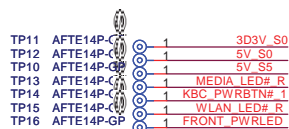
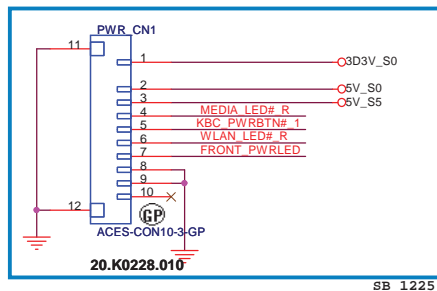
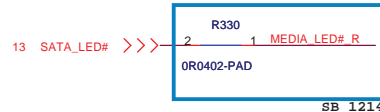
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Title			
NONE BOARD			
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LED

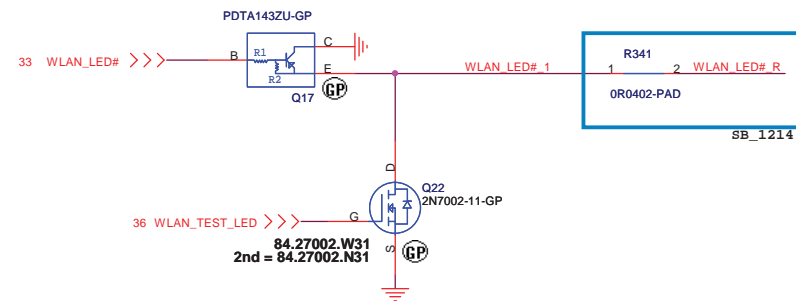
FRONT_PWRLED# Q 1 R604
STDBY_LED# Q 1 R618
DC_BATFULL# Q 1 R605
CHARGE_LED# Q 1 R617

FRONT_PWRLED# Q 1 DY EC58
STDBY_LED# Q 1 DY EC61
DC_BATFULL# Q 1 DY EC57
CHARGE_LED# Q 1 DY EC60



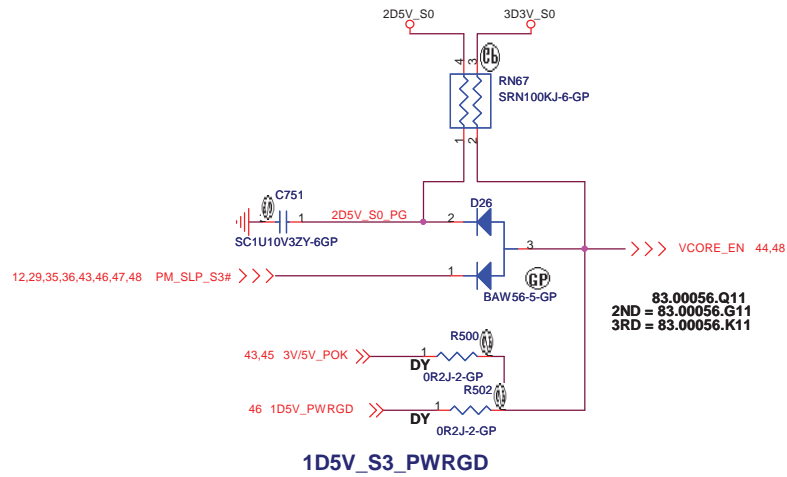
Power LED

Charger LED

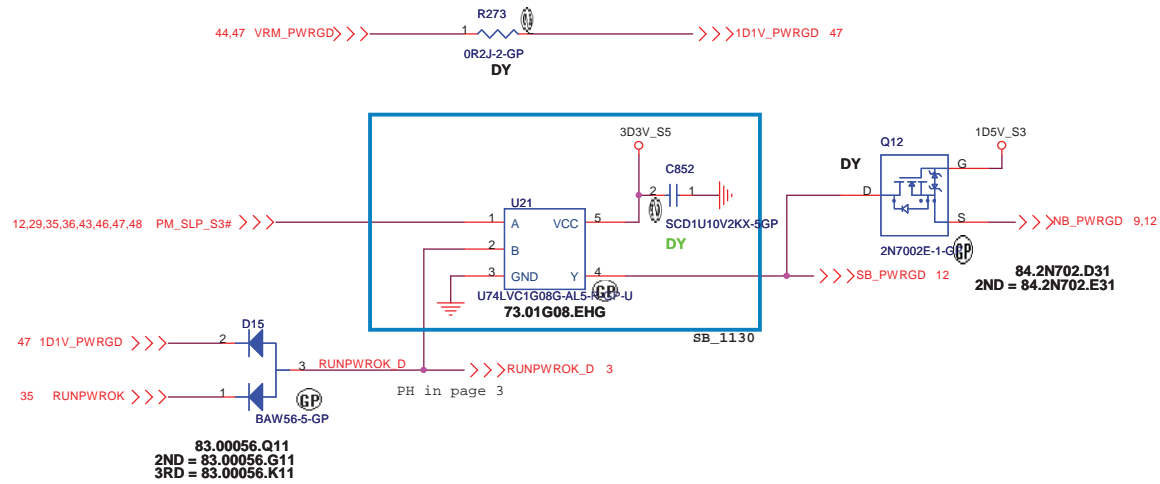


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Taipei Hsien 221, Taiwan, R.O.C.

Title			LED
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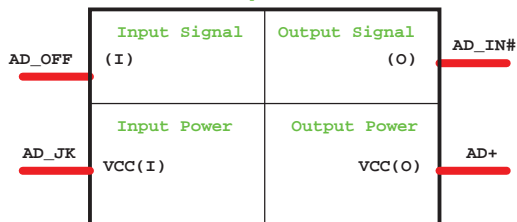


P/H @ 1D8V_S3 PAGE

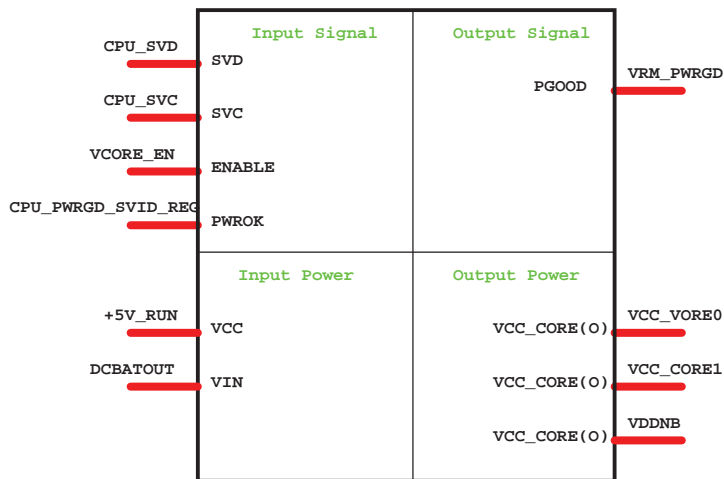


JE70-DN

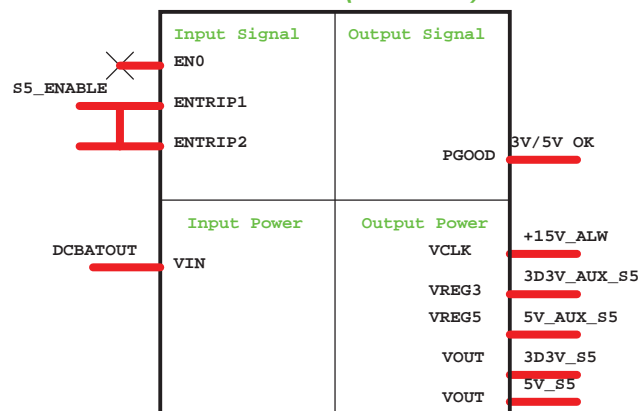
Adapter



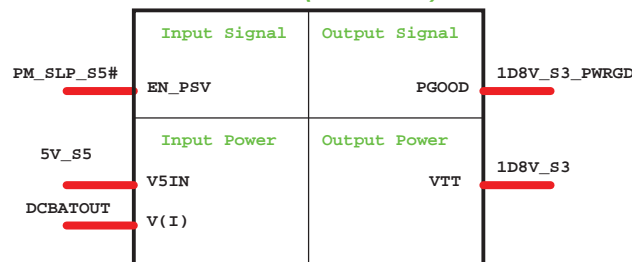
CPU_CORE ISL6265HRTZ



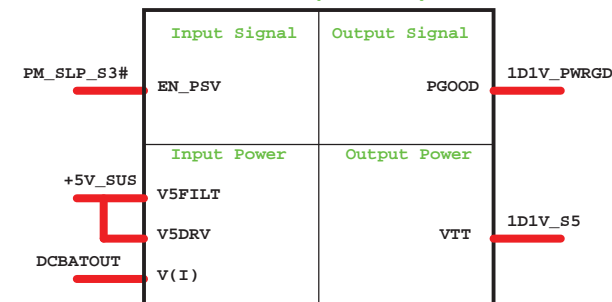
DCDC 5V/3D3V(RT8205A)



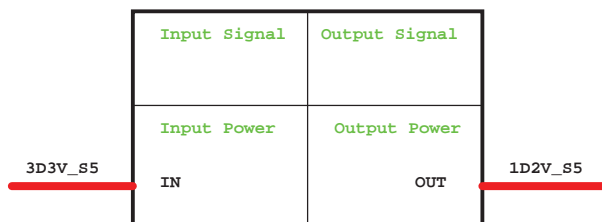
DCDC 1D8V(RT8209B)



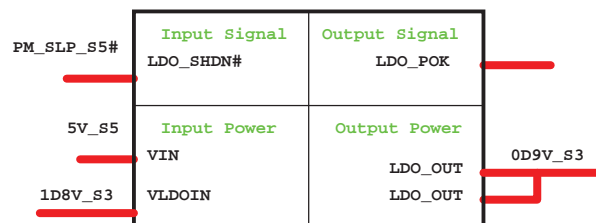
DCDC 1D1V(RT8209)



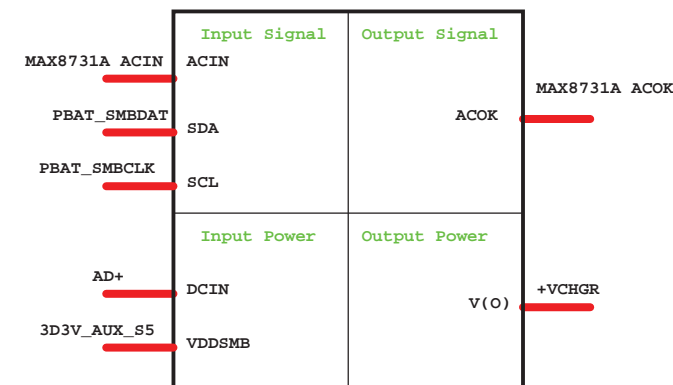
1D2V LDO G9161



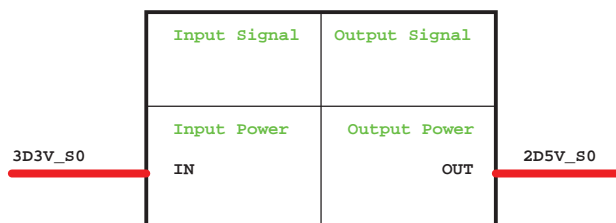
0D9V LDO RT9026



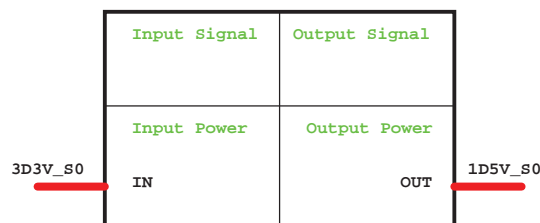
CHARGER MAX8731



2D5V LDO R9161



1D5V LDO G9571

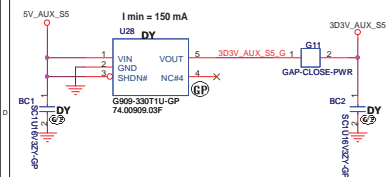


JE70-DN

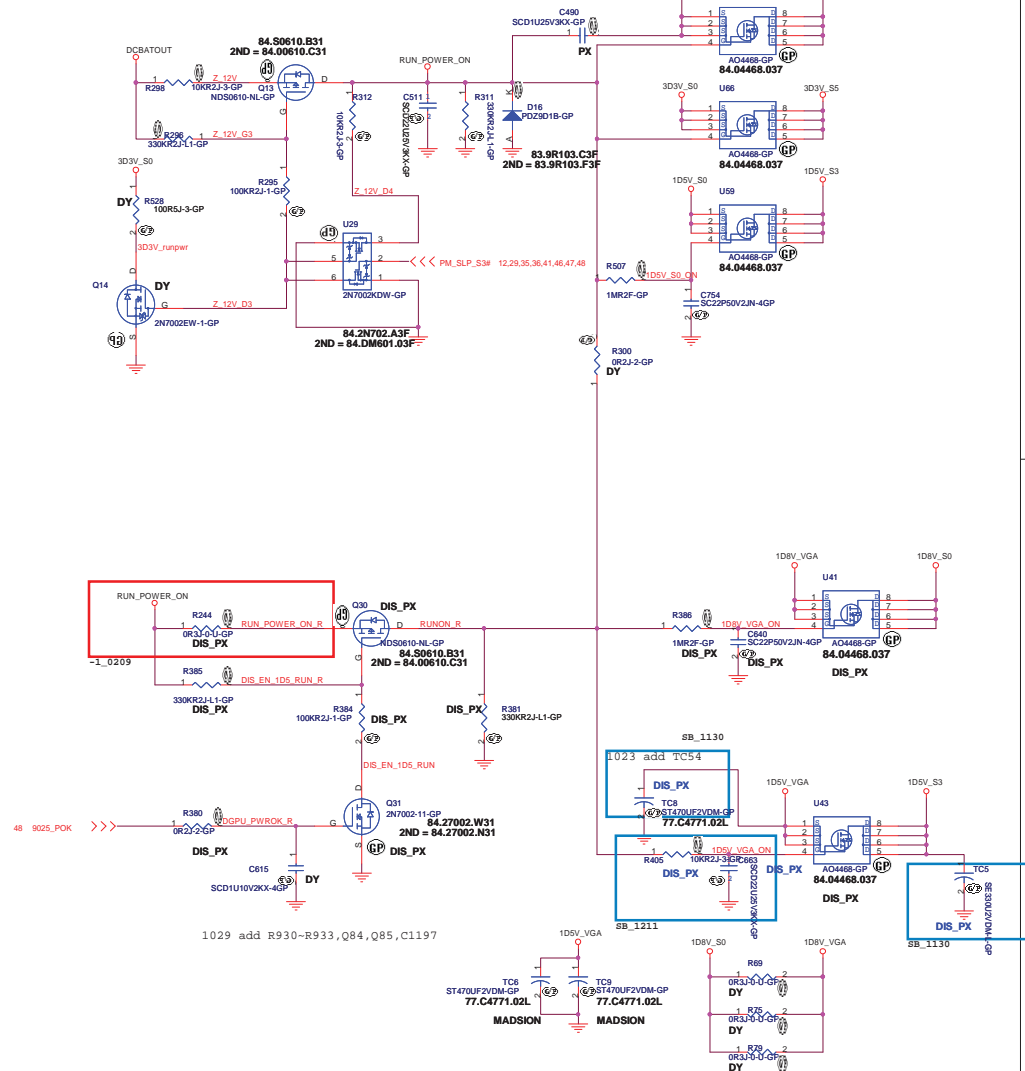
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			Power Block Diagram		
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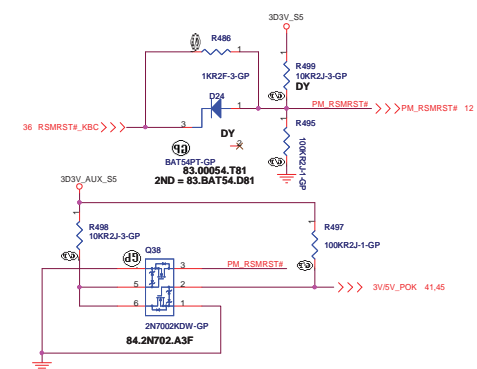
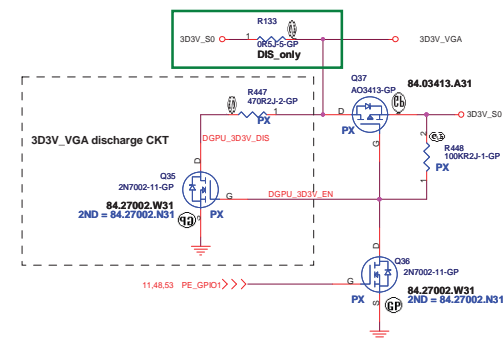
Aux Power 3D3V_AUX_S5

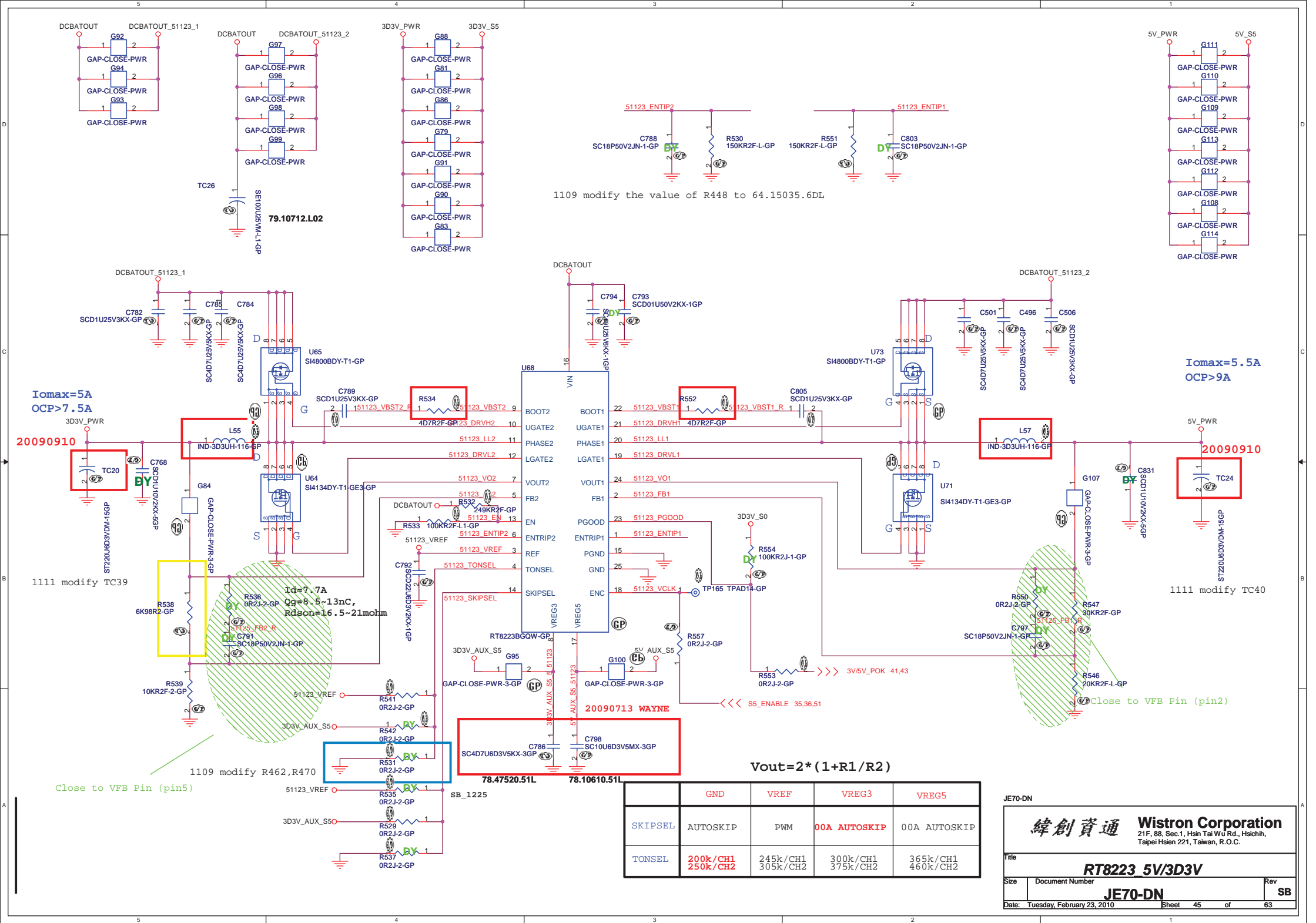


Run Power

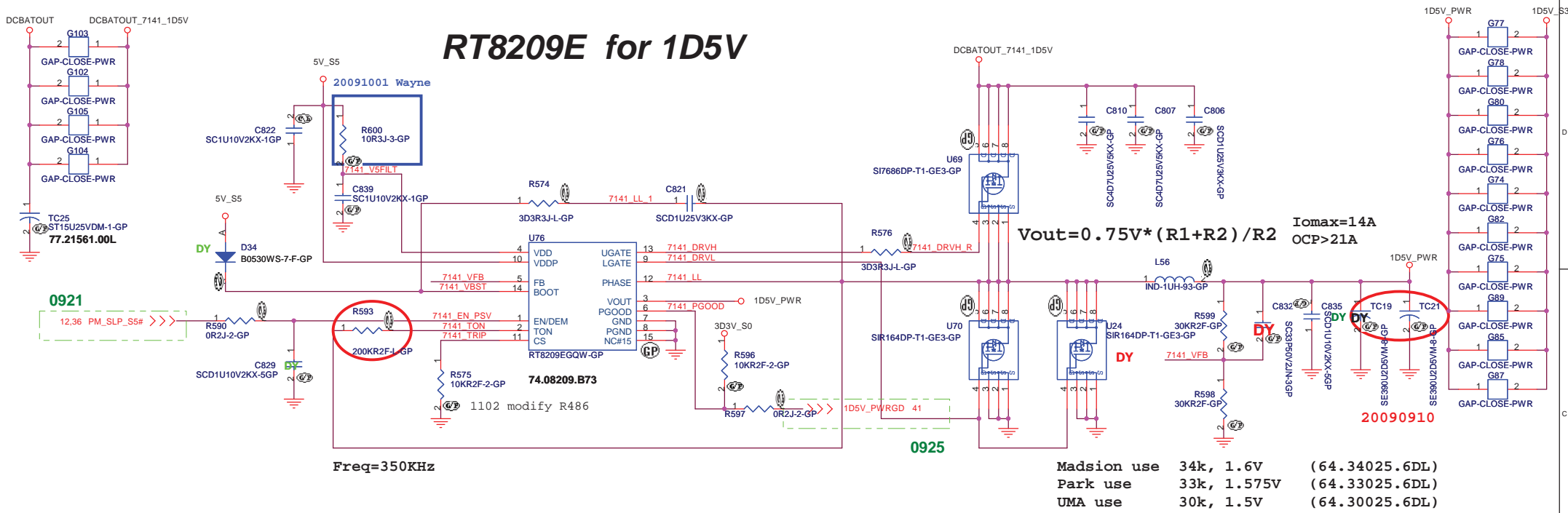


+3VS to 3.3V_DELAY Transfer

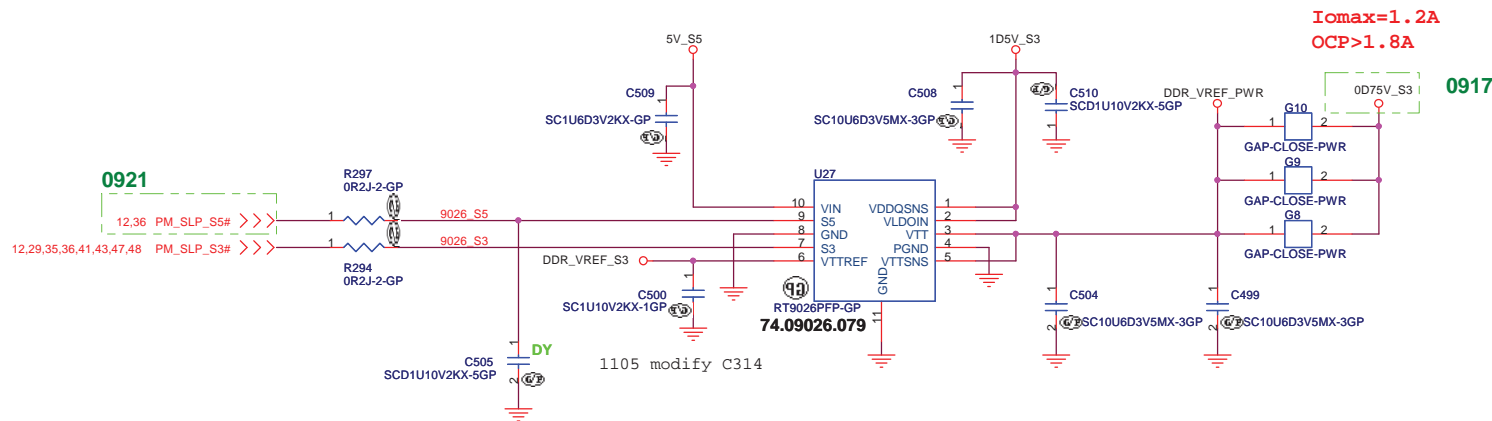




RT8209E for 1D5V

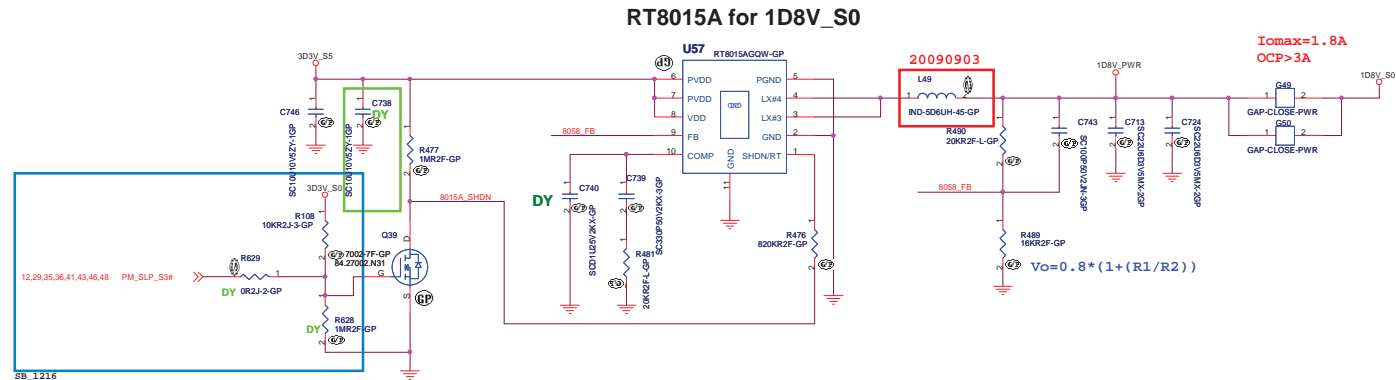
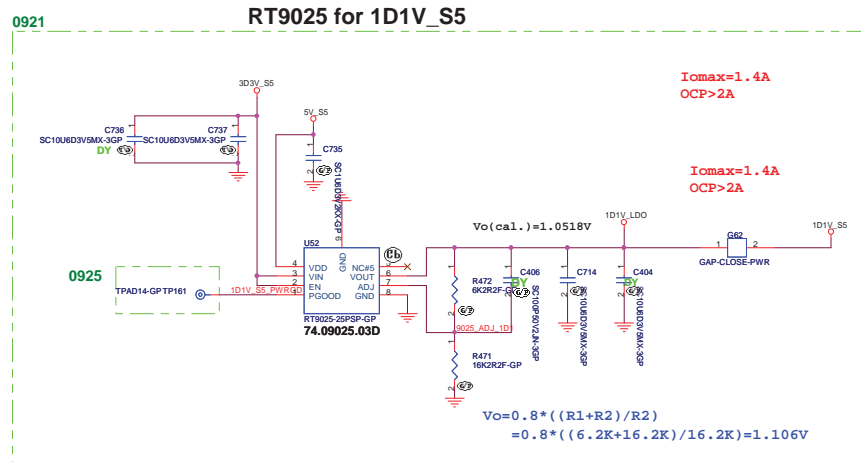
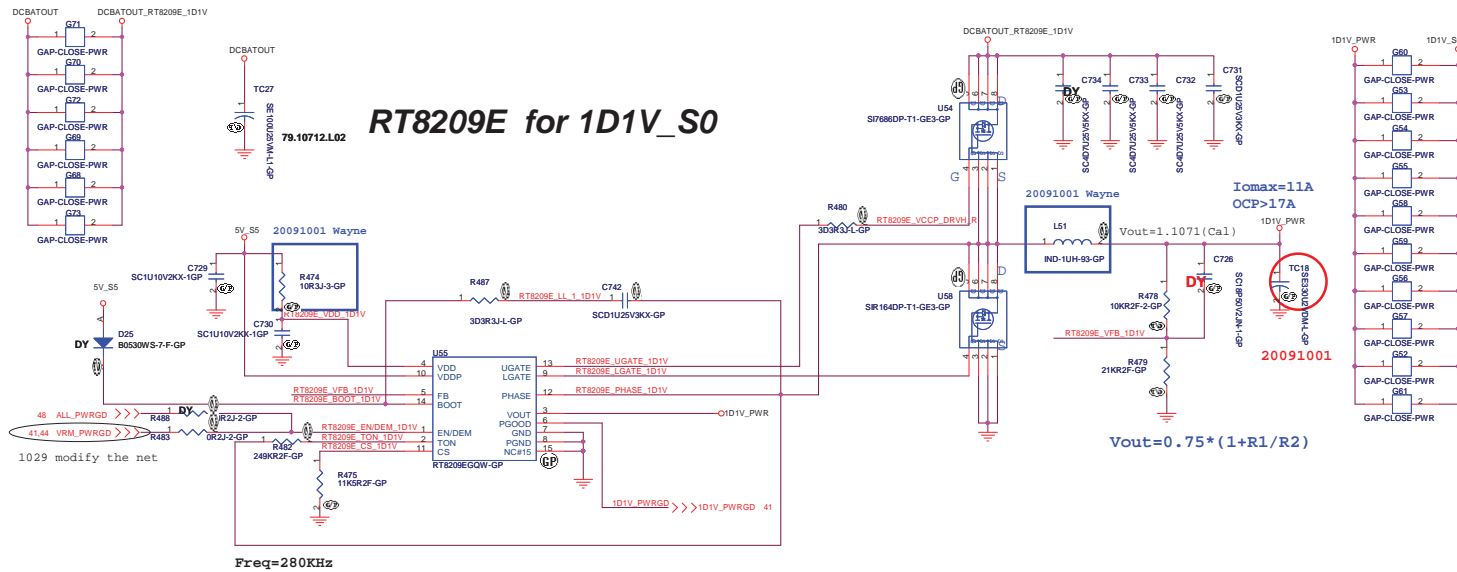


RT9026 for 0D75V_S3



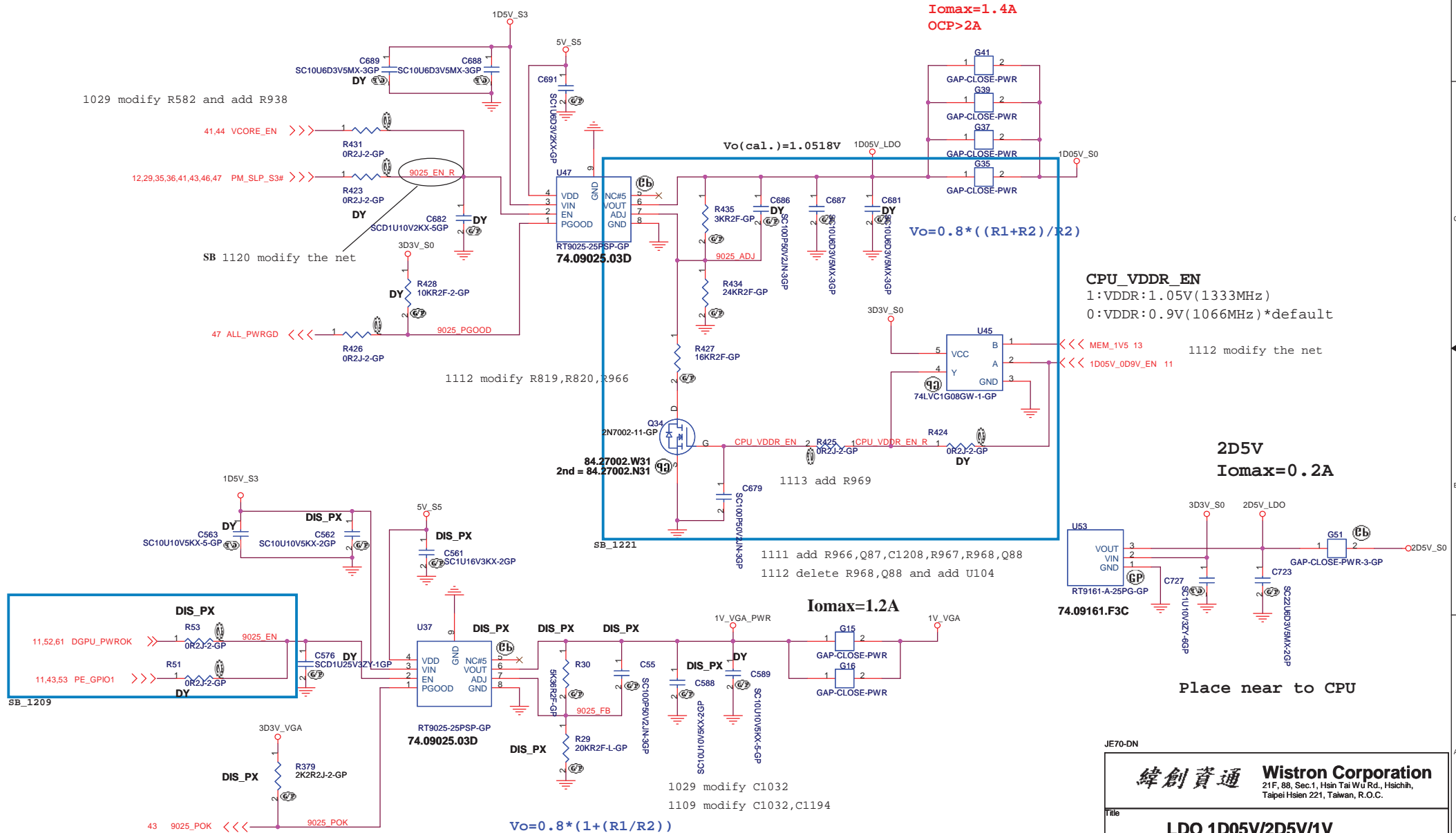
JE70-DN

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Title: RT8209E 1D5V	
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RT9025 for 1D05V_S0

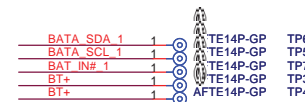


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Title		
LDO 1D05V/2D5V/1V		
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1021 modify DCIN1
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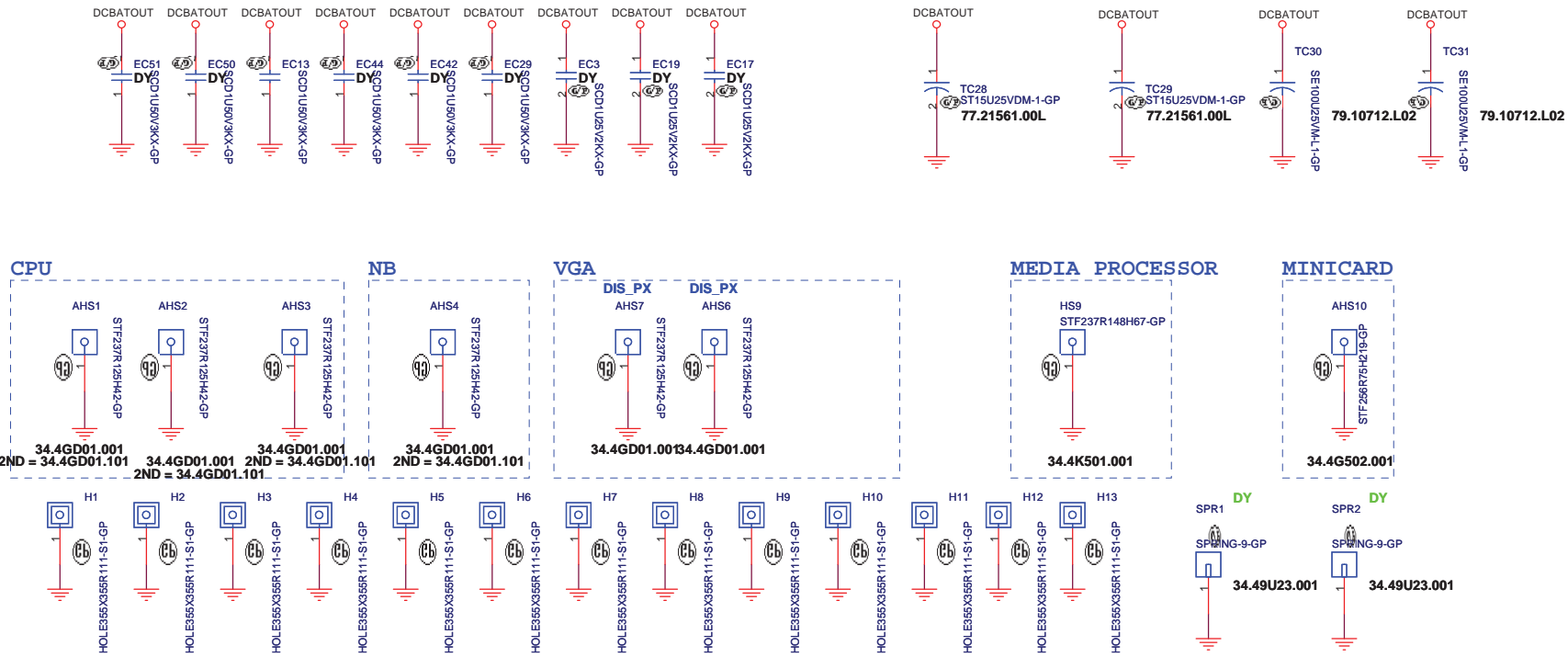


Pin NO	Symbol
1	GND
2	GND
3	SMD
4	SMC
5	TS
6	B/I
7	BT+
8	BT+

JE70-DN

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Title			
AD/BATT CONN			
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Check test point

3D3V_S0		TP171	TPAD14-GP
3D3V_AUX_S5		TP170	TPAD14-GP
3D3V_S5		TP172	TPAD14-GP
5V_S5		TP167	TPAD14-GP
12,36 PM_PWRBTN#	<<<	TP169	TPAD14-GP
6,11 CPU_PWRGD	<<<	TP163	TPAD14-GP
35,36,45 SS_ENABLE	<<<	TP173	TPAD14-GP
6,11 CPU_LDT_RST#	<<<	TP162	TPAD14-GP

Test Point放在Dimm Door打開可量測處

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緯創資通

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Title

EMI/Spring/Boss

Size

Document Number

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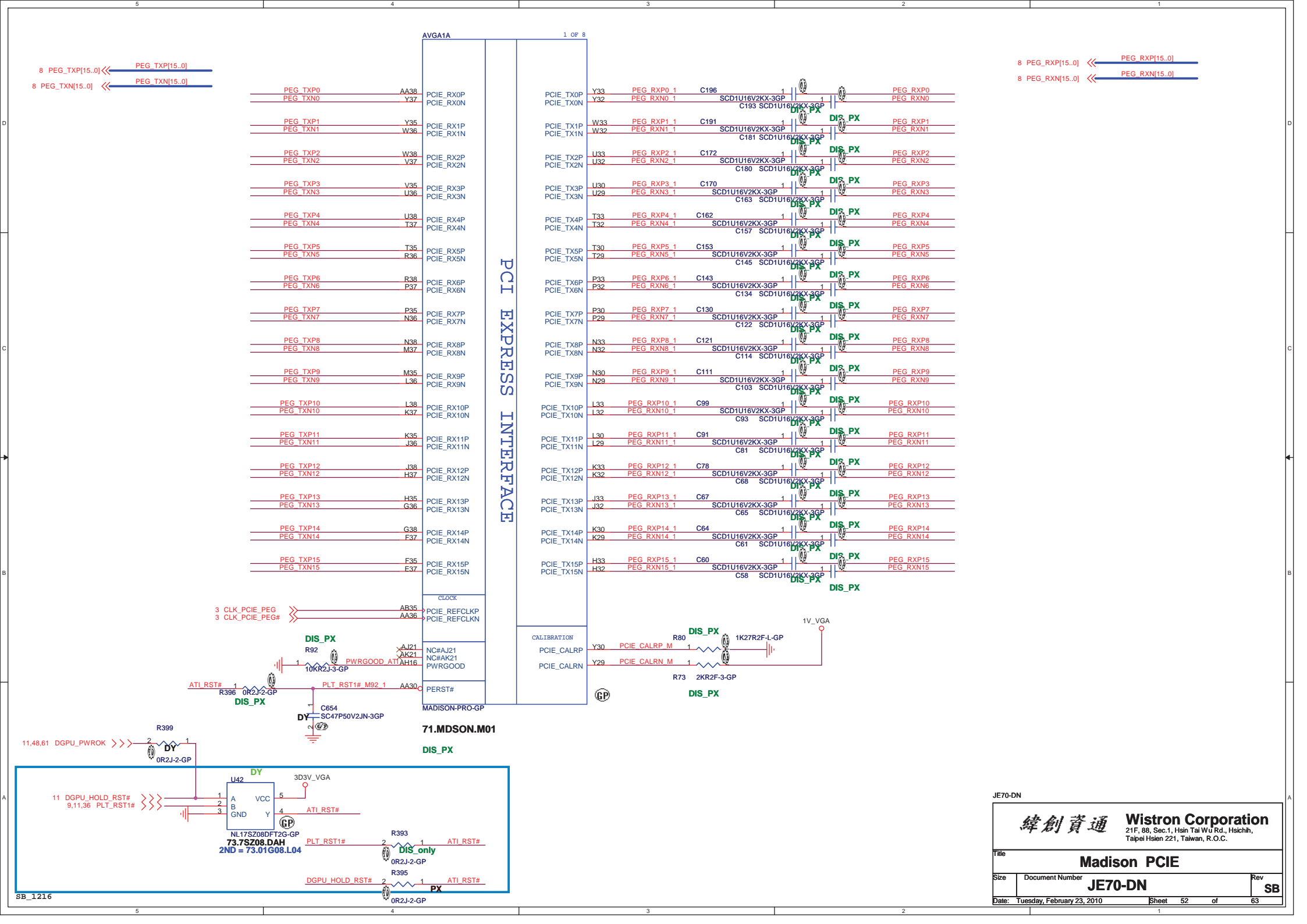
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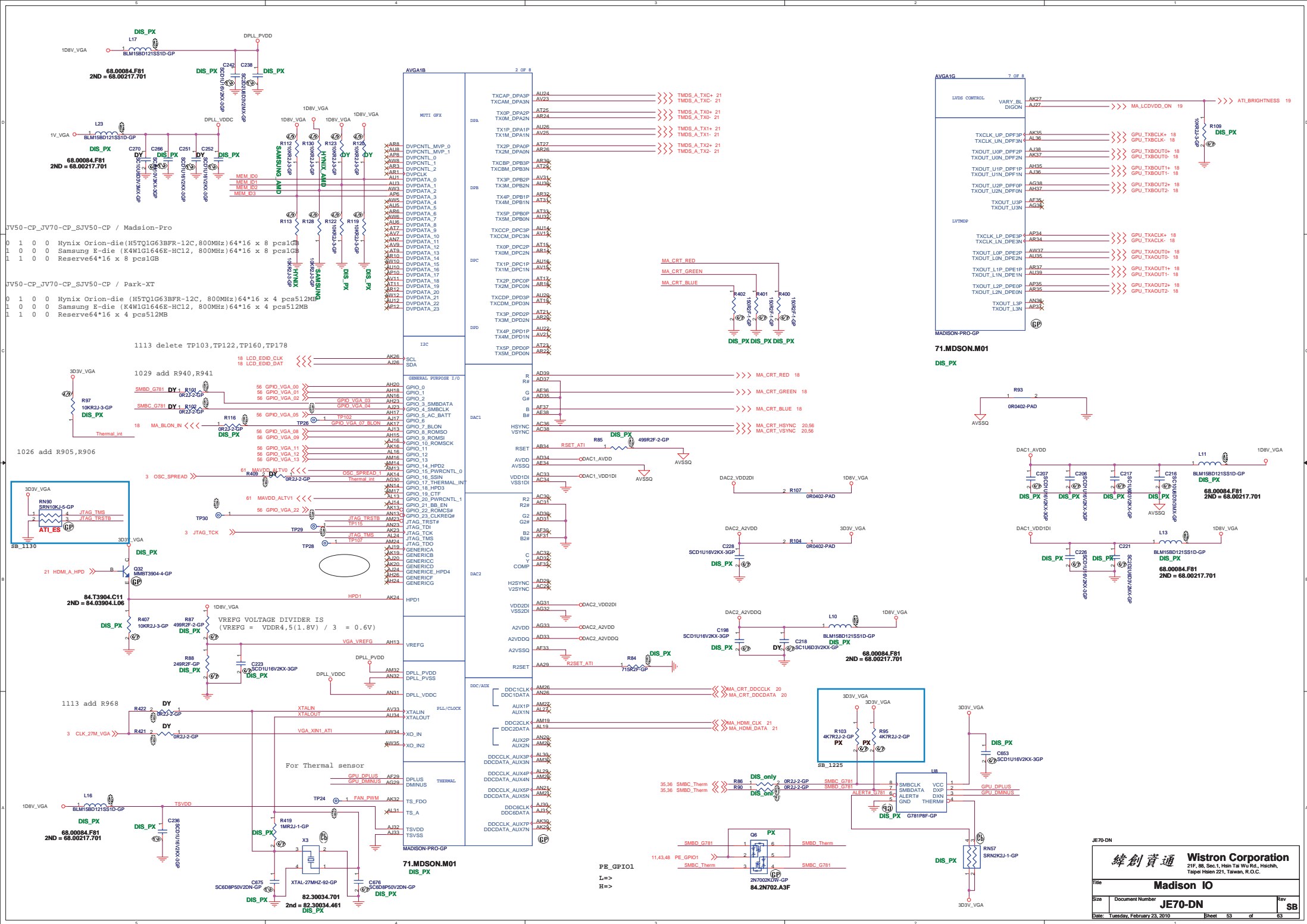
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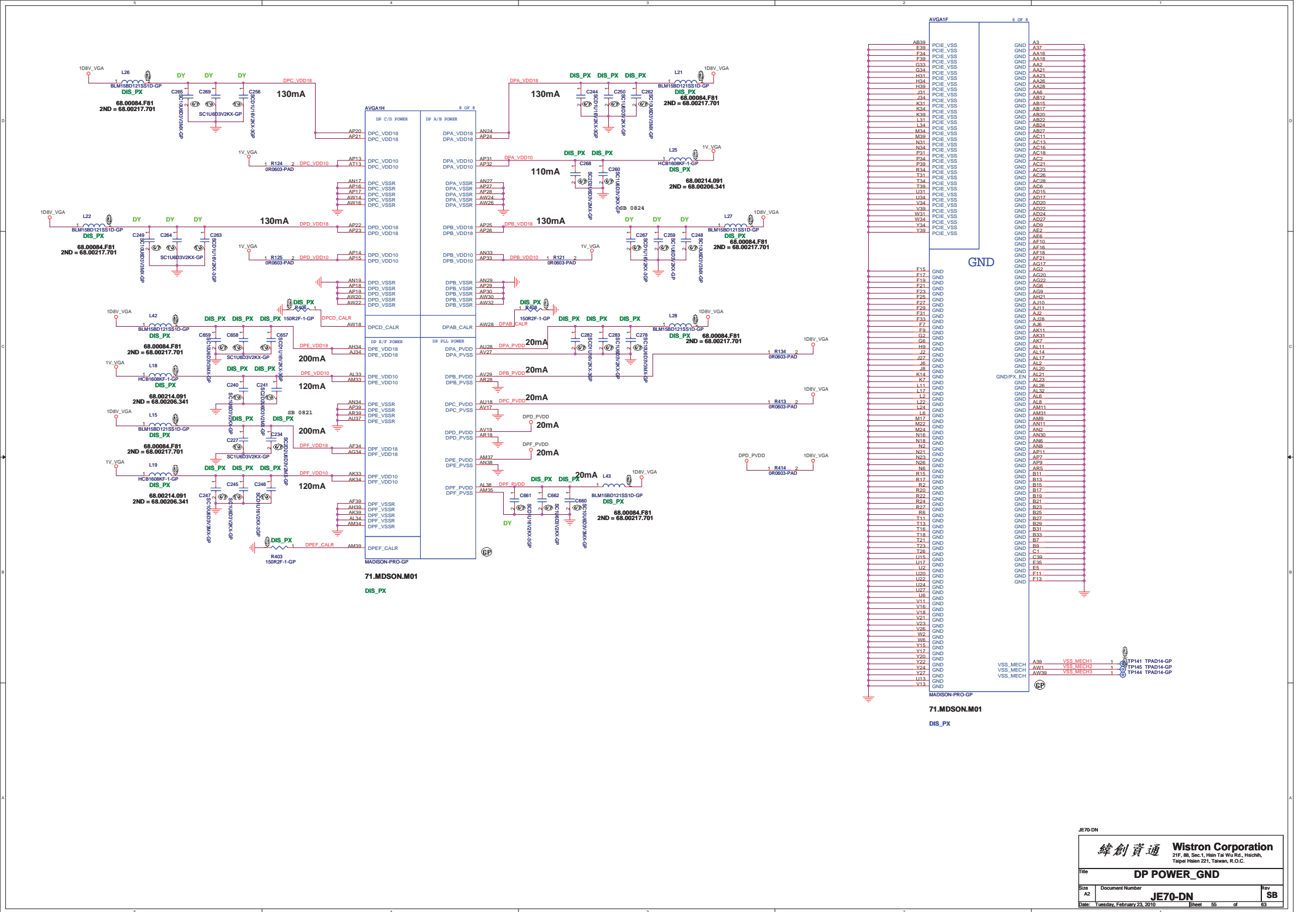
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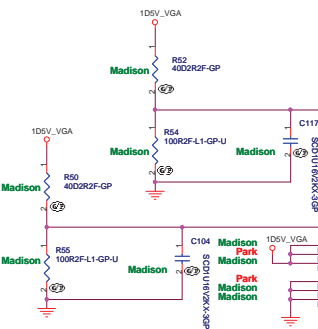






For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRP1 are used

71.MDS0N.M01

DIS_PX

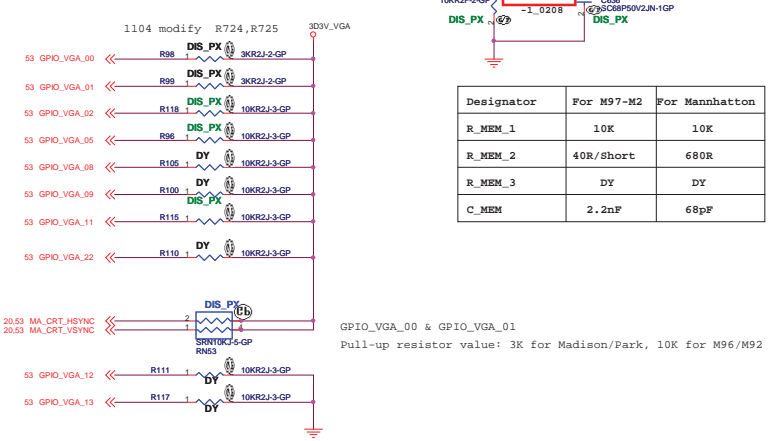
STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT N= NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIe Full Tx Output Swing Transmitter Power Savings Enable 0= Full Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00: No audio function 01: Audio for DisplayPort and HDMI 1: if adapter is detected 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

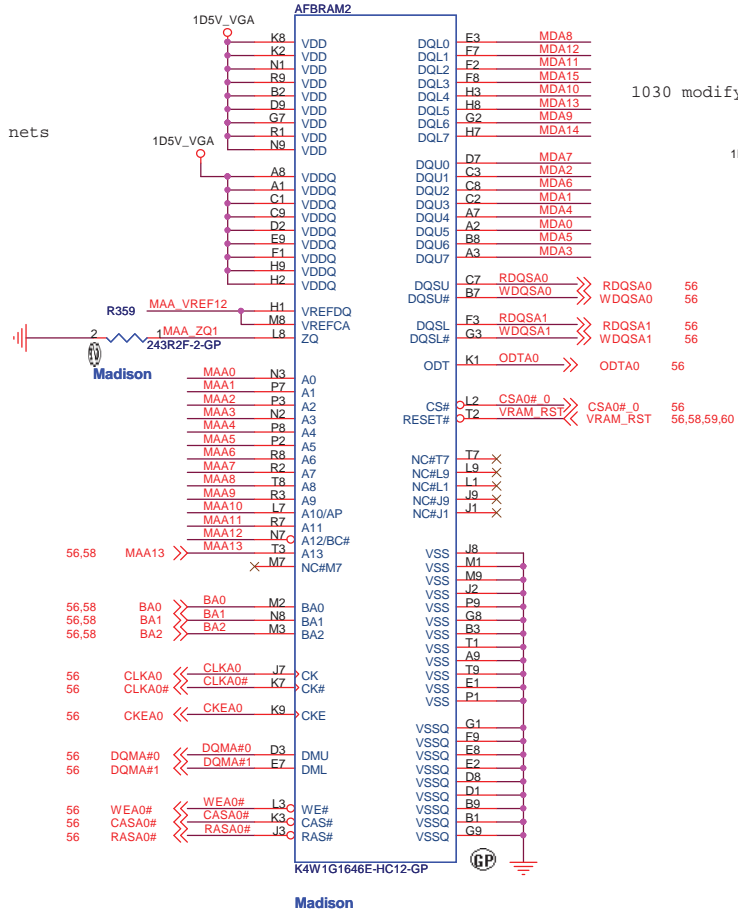
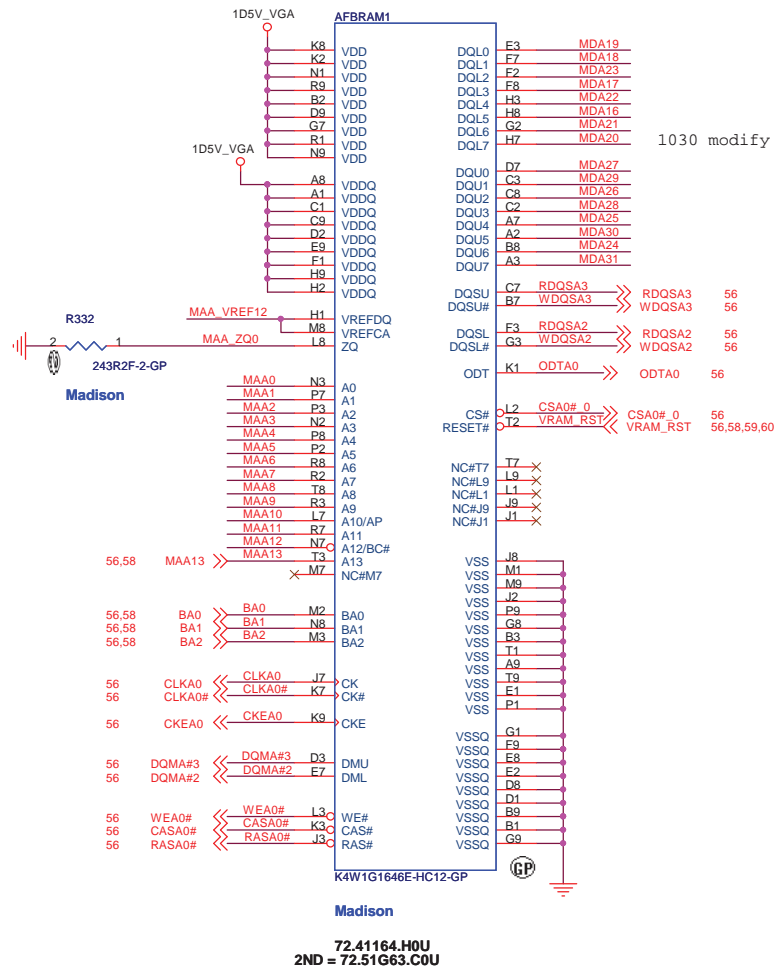
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICCC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1	
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number
128MB	x000		M25P05A 0100
256MB	x001	ST Microelectronics	M25P10A 0101
64MB	x010		M25P20 0101
32MB	x		M25P40 0101
512MB	x		M25P80 0101
1GB	x		
2GB	x	Chingis (formerly PMC)	Pm25LV512A 0100
4GB	x		Pm25LV010A 0101

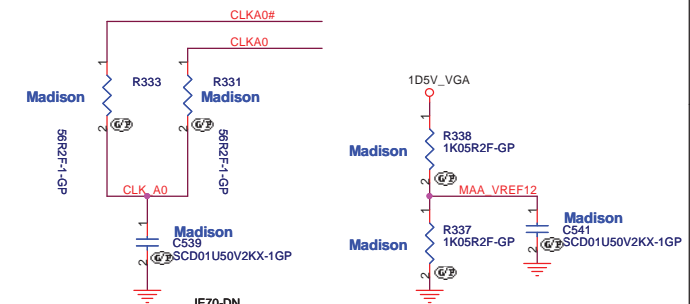
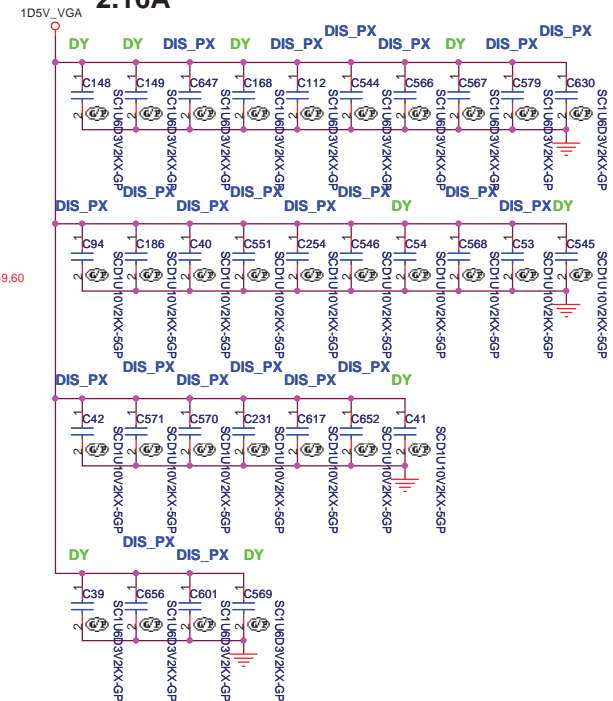


DDR3

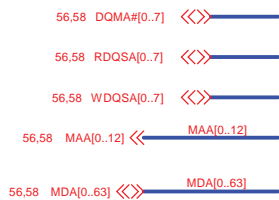


```
1030 modify these nets
```

2.16A



```
SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX:   72.51G63.C0U(VR.1GB0G.004)
```



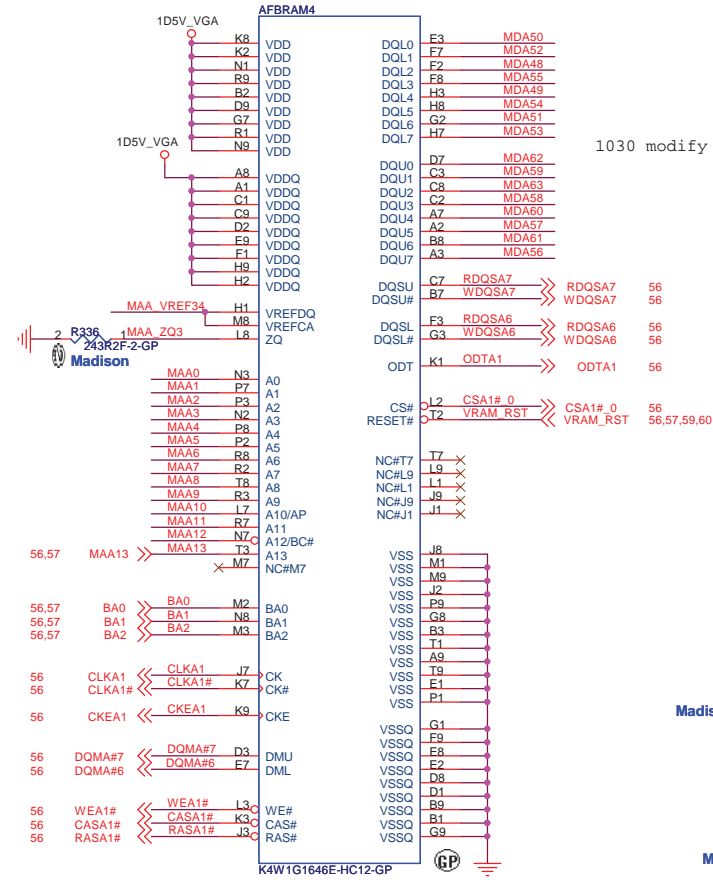
DDR3



Madison

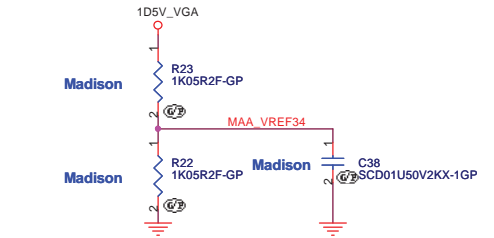
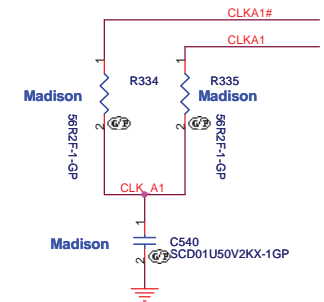
72.41164.H0U
2ND = 72.51G63.C0U

SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)



Madison

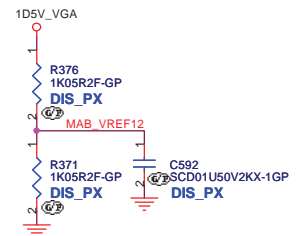
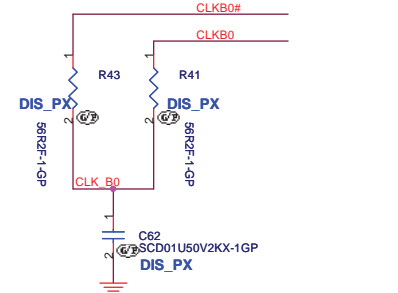
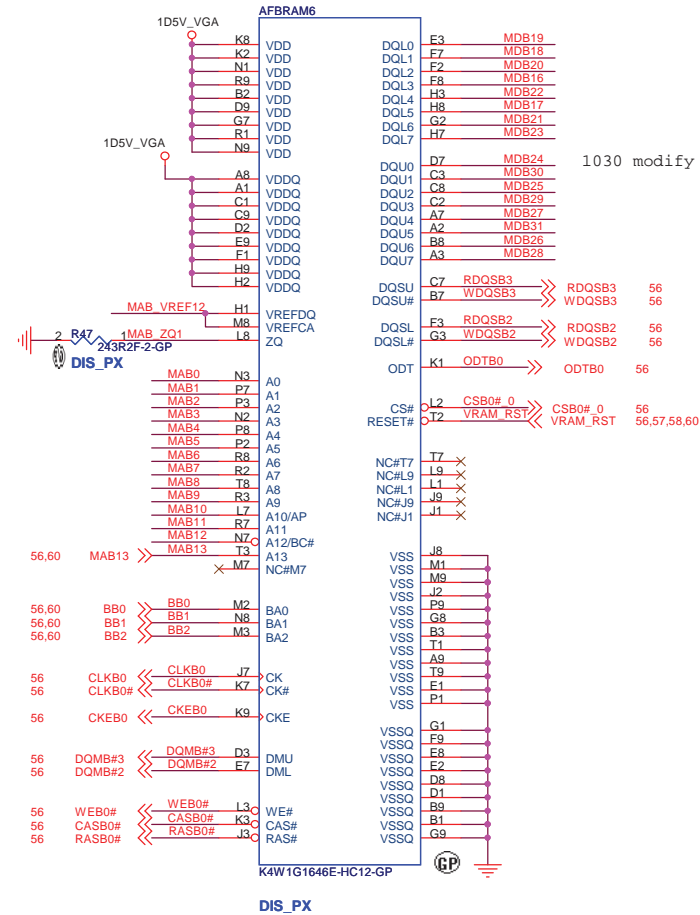
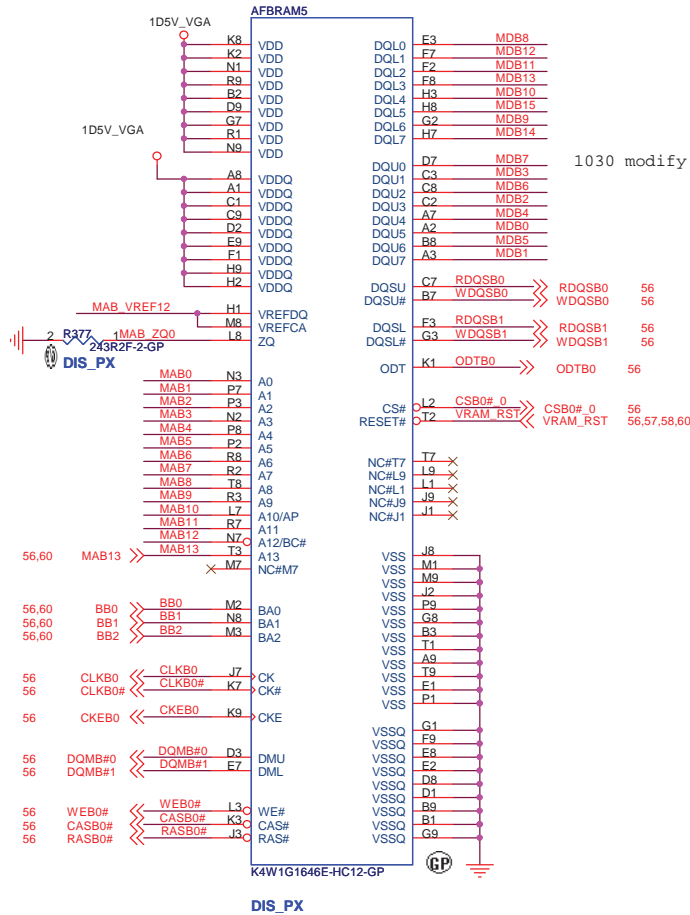
72.41164.H0U
2ND = 72.51G63.C0U



JE70-DN

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
VRAM(2/4)	
Size	Document Number
A3	JE70-DN
Date: Tuesday, February 23, 2010	Sheet 58 of 63
Rev	SB

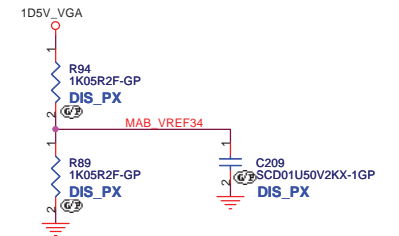
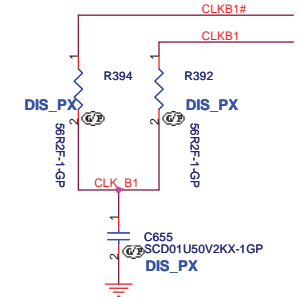
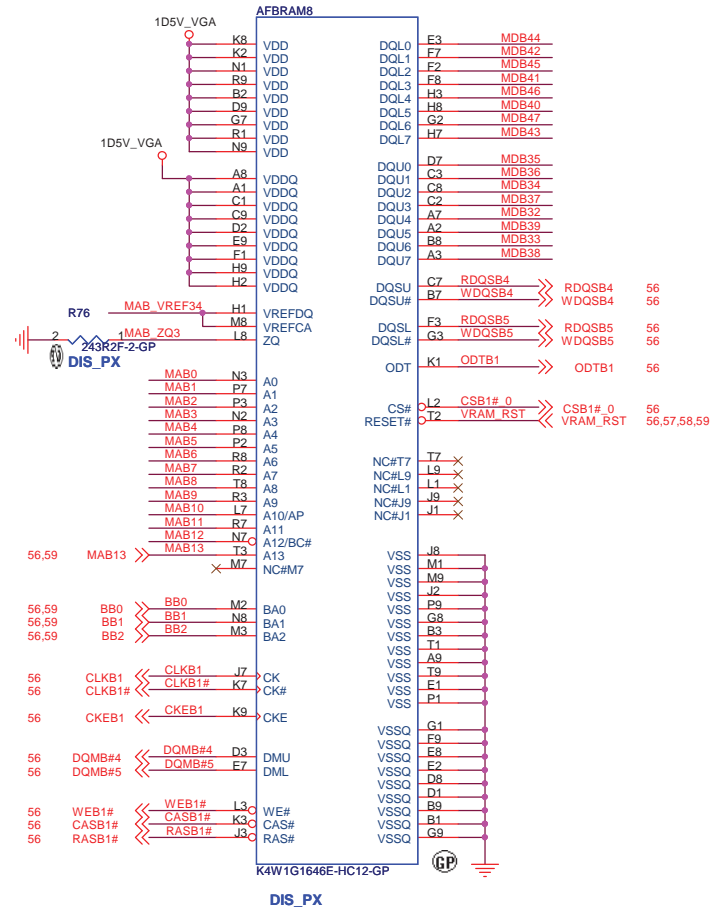
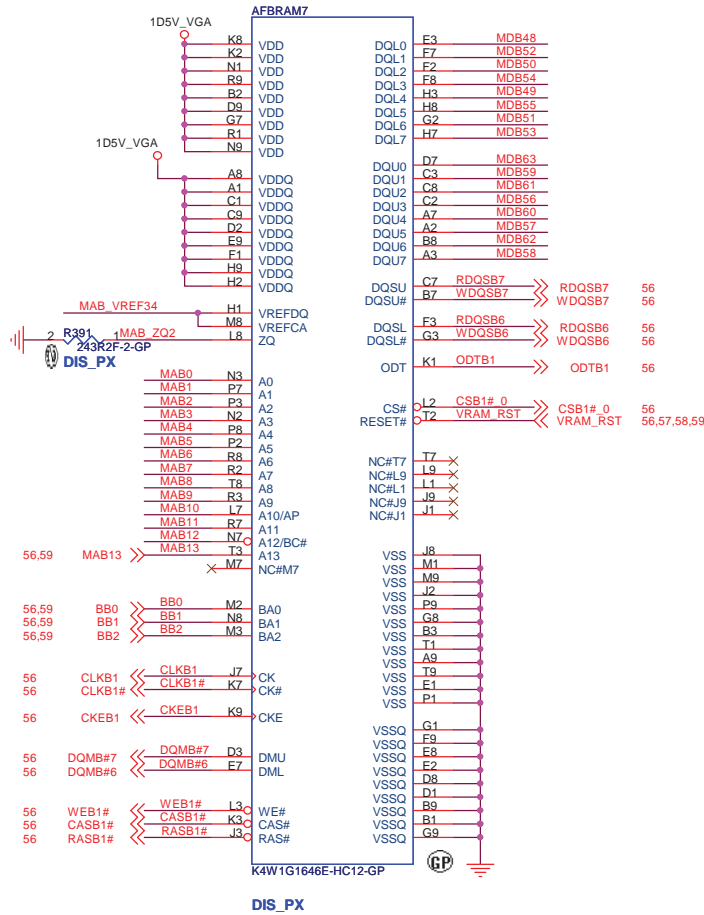
DDR3



JE70-DN

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Title		
VRAM(3/4)		
Size	Document Number	Rev
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DDR3



56,59 DQMB#[0..7] <<>>

56,59 RDQSB#[0..7] <<>>

56,59 WDQSB#[0..7] <<>>

56,59 MAB#[0..12] <<>>

56,59 MDB#[0..63] <<>>

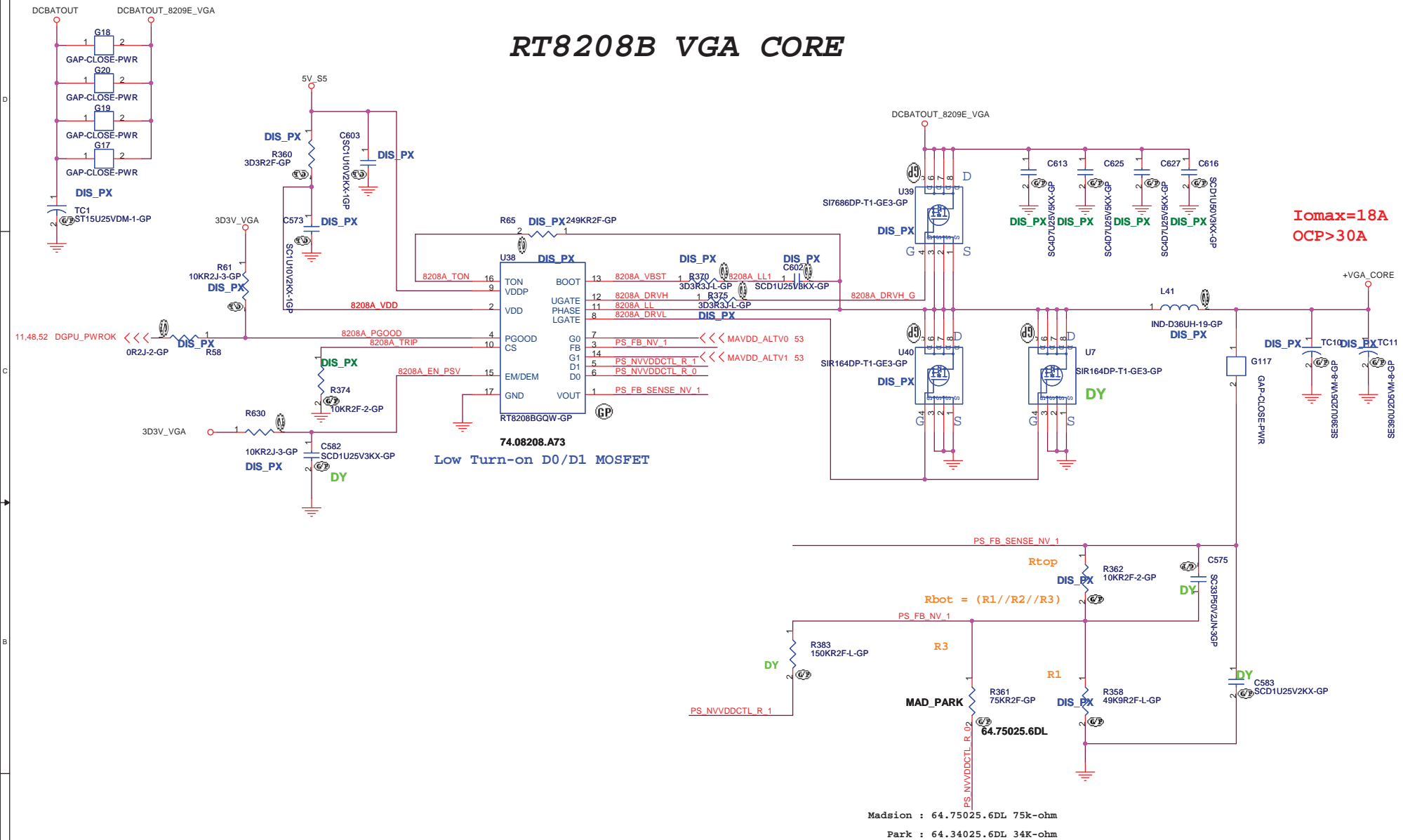
SAMSUNG: 72.41164.H0U(VR.1GB0B.006)

HYNIX: 72.51G63.C0U(VR.1GB0G.004)

JE70-DN

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
VRAM(4/4)			
Title	Size	Document Number	Rev
	A3	JE70-DN	SB
Date: Tuesday, February 23, 2010	Sheet	60	of 63

RT8208B VGA CORE



MAVDD_ALTVO	Madison Pro	Park XT
0	1.00V	1.12V
1	0.90V	0.90V

JE70-DN

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
RT8209E VGA CORE			
Size A3	Document Number		Rev
	JE70-DN		SB
Date:	Monday, March 01, 2010	Sheet 61 of 63	

1020

Page8: modify these nets for PCIE ports
Page11:add these nets(INT_VGA_EN#,EDP_EN)
Page11:add the net(PX_EN#) and R861
Page11:delete D41,R437,R435
Page12:modify these nets for USB ports
Page14:modify L45,L48,L52,L57,L58,L60
Page18:delete RN95,R423 and add Q73-Q76,R862-R864,D45
Page19:delete CCD1 conn and modify these nets for CCD
Page19:add R865,R866,U100
Page20:add Q77,R867
Page24:add modify these nets for BT
Page25:add modify these nets for USB board
Page26:modify these nets for PCIE port(LAN)
Page26:delete the net(LOW_PWR)
Page33:modify these nets for PCIE ports(MINI1,MINI2)
Page33:modify these part's names
Page33:modify these nets for USB port(MINI2)
Page40:1020 modify PWR_LED1,CHARGER_LED1
Page51:add screw holes

1021

Page5:modify these nets
Page6:delete HDT1 conn and add TP246~255
Page16:modify these nets of ADM1
Page16:add R880~883
Page17:modify these nets of ADM2 and ADM3
Page17:add R884-R891
Page18:add RN114~117
Page23:modify ODD1
Page25:modify the net(COVER_SW#_1)
Page30:modify LOUT1,AMIC1 and MICIN1
Page33:modify AMIN11 and MINI2
Page36:modify these nets and add R873-878
Page38:modify these devices(ATPCN1,SW_R,SW_L)
Page40:modify PWR_LED1,CHARGER_LED1
Page49:add D46
Page50:modify DCIN1, BAT1 and add R879

1021

Page26:modify U6(LAN IC)

1023

Page12:delete R538,R539 and add RN118
Page12:delete R442,R443,R445 and add RN119
Page12:delete R570-R572 and add RN120
Page12:delete C368-C371,C446,C449,C686,C687
Page18:swap these nets
Page21:add R892-R900,Q78
Page25:delete TC29,TC24,EC79,EC83
Page25:modify the net of USBCN1 pin32
Page36:delete R258 and RN89,RN122
Page36:delete R382 and add U101
Page36:delete R892,R483,R497,R478 and add RN123
Page36:delete R410,R416 and add RN121,R892
Page37:add R901,R902
Page40:modify the pin5 define of PWR_CN1 and Q11
Page43:add TC53,TC54,U44
Page61:modify TC52, R295 and add R903,Q79

1026

Page3: add R904 and modify C509,R232,R235
Page6: add R913,RN124
Page6: modify RN42,RN84,R612,R611,R364
Page17:modify these nets
Page19:modify R588
Page21:modify U73 and delete R504
Page22:modify SATA1
Page35:delete R311 and modify FAN1
Page36:modify RN121
Page36:modify AKB1
Page37:modify RN94 and the net(SPI_WF#)
Page43:add R097-R911,D47,Q80
Page53:add R905,R906

1027

Page10:delete C651,R320,R316
Page11:modify C543,C306,C424,C433
Page11:delete R148
Page12:modify the net(PM_RSMRST#)
Page43:modify the net(PM_RSMRST#)

1028

Page3:add the net(LAN_CLKREQ#) to RN70
Page4:modify C704-C706
Page4:modify R401
Page9:delete R576,R578
Page10:modify C62,C91
Page11:delete R207,C337,D5,R208
Page11:delete the net(PCI_REQ#6)
Page12:delete RN120 and add R570
Page13:modify the net(SATA_LED#)
Page14:add C1198,C1199 and modify C815,C811
Page16:add R934,R935
Page18:add U102,R915-R919
Page18:modify R432,U3,U8
Page19:add U103,R920-R922 and delete D35
Page20:add R936,R937 and modify R325,R323,R354
Page21:delete RN8,RN13,RN15,RN19
Page21:modify C819-C821,C823,C824,C826-C828
Page25:add L82,R924,R925
Page29:modify R489
Page30:modify R622,R619 and add RN125
Page36:delete R384 and modify the net(KBC_BL_ON_IN)
Page36:add R926
Page43:delete R583,D33,U74,R340,Q34,R584
Page43:add R930-R933,Q84,Q85,C1197
Page43:add R927-R929,Q8-Q83
Page43:delete R591-R595
Page48:modify these nets(DGPU_PWROK,9025_POK)

1029

Page6:delete R364,R612 and add RN127,R946
Page16:delete C331,C338
Page17:delete C348,C340,C350,C342
Page18:modify these nets
Page19:add EC99,EC100
Page24:add EC101,EC102
Page25:add L82,R924,R925,R939,EC103
Page35:delete D17,D18,U39,U43,R298,R322,R330,R338,R337,C646,C656
Page35:delete U38,R321,R308,R309,R314,C645
Page36:add R945,RN126
Page43:delete U44,R342,C675
Page47:modify the net
Page48:modify R582 and add R938
Page50:add D48
Page53:add R940-R943
Page61:add R944,Q86

1030

Page3:modify these nets
Page8:modify these nets
Page11:modify the net
Page12:add R949
Page14:delete C760,C721,C805,C800,C769,L64 and add R948
Page18:modify these nets
Page30:add R950-R953 and modify EC24,EC51
Page57:swap these nets
Page58:swap these nets
Page59:swap these nets
Page60:swap these nets

1102

Page3:swap these nets
Page6:swap these nets
Page12:swap these nets
Page13:swap these nets
Page18:swap these nets
Page25:modify USBCN1
Page30:modify these names of these nets

1103

Page3:modify X5,C508,C509
Page11:modify R164
Page14:modify L51,L59
Page21:modify these names of nets
Page21:add RN8,RN13,RN15,RN19
Page36:add the net(A_MIC_SUPPORT#)

1104

Page6:delete TP246-255 and add HDT1
Page9:modify the value of RN11
Page24:add AFTP(TP256-TP258)
Page24:add AFTP(TP259-TP263)
Page25:add AFTP(TP264-TP280)
Page35:add AFTP(TP281,TP282)
Page36:add AFTP(TP283-TP307)
Page38:add AFTP(TP308-TP312)
Page40:add AFTP(TP313-TP319)
Page56:modify these values of R724,R725

1105

Page3:delete R191-R194,R198-R200,R204-R206
Page3:delete R214,R213,R187-R190,R220,R222
Page3:add RN128-RN136
Page3:modify R215,R197,R238,R229
Page6:delete R104,R105,R108,R110
Page6:add RN137,RN138,R954
Page6:modify R366
Page6:modify Q8,R81,R375,C205
Page8:delete TP16,TP17,TP20,TP21
Page9:add R955,R956 and modify R29
Page11:delete R144,R141,R137,R138
Page12:add the net(SUS_STAT#) and R957
Page12:modify these nets
Page21:swap these nets
Page28:modify C713,R634 and delete R626
Page33:modify these nets
Page33:modify R879

1106

Page3:modify these values of R169,R170
Page12:add R957,R958
Page12:add these nets(USB_OC#0,USB_OC#2,USB_OC#3)
Page16:modify R880-R883,ADM1
Page17:modify R888,R890,ADM2
Page21:add R959
Page35:modify FAN1
Page35:modify PWR_CN1
Page35:modify ATPCN1
Page36:swap these nets(KBRCIN#,KA20GATE)
Page37:swap RN94
Page44:swap RN45
Page51:add EC104-EC112 for EMI demand

1107

Page3:swap RN129,RN130,RN132
Page6:swap RN137
Page51:add EC104-EC112 for EMI demand

1109

Page45:modify the value of R448 to 64.15035.6DL for Power team demand
Page45:modify R462,R470 for Power team demand
Page46:modify L25 for Power team demand
Page48:modify C1032,C1194

1110

Page5:swap RN48
Page7:add C1200-C1207
Page11:add R960,R961
Page25:modify USB1
Page43:add TC55,TC56
Page52:add R962

1111

Page11:add R965
Page21:modify HDM11
Page28:add R626
Page33:delete C550,C549 and add R963
Page36:delete RN121 and add R964
Page45:modify TC39,TC40
Page48:add R966,Q87,C1208,R967,R968,Q88

1112

Page13:modify the net
Page48:delete R968,Q88
Page48:modify R819,R820,R966
Page48:modify the net

1113

Page3:delete R170,EC50
Page25:delete R939,TP272,EC103
Page46:modify TC43
Page48:add R969
Page53:add R968
Page53:delete TP103,TP122,TP160,TP178
Page53:delete these TP(TP157,TP145...))
Page54:delete TP3-TP9

1117(Rename)

Page18:swap these nets
Page22:delete D29-D31,D33
Page36:modify RN31
Page61:delete G24-G29
Page61:modify the net

1118

Page14:add R620 and modify R184
Page15:modify R412,R411
Page36:swap AKB1 pin1-pin26

JET0-DN

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
HISTORY(1/2)			
Size	Document Number	Rev	SB
K2			
Date: Thursday, November 19, 2009		Sheet	62 of 63

SA to SB

1120

Page19: modify these nets
Page48: modify the net(9025_EN)

1124

Page38: modify ATPCN1

1126

Page25: modify these nets
Page36: add TP174